AMD

MACH™ Family Data Book

1991

MACH™ Family Data Book

High Density EE CMOS Programmable Logic

Includes Final Commercial Data Sheets for the MACH110 & MACH210

Advanced Micro Devices

MACH™ 1 and MACH 2 Families

High Density EE CMOS Programmable Logic

Q2 1991 Data Book

Final:

MACH110 Com'l
MACH210 Com'l

Preliminary:

MACH110 Mil
MACH120 Com'l
MACH130 Com'l, Mil
MACH210 Mil
MACH230 Com'l, Mil

Advance Information

MACH220 Com'l

ADVANCED MICRO DEVICES

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If you have always wanted higher-density EE CMOS PAL® devices, with no penalty in speed or cost per function, this booklet will help you a lot!

We have taken our high-volume 0.8-micron EE CMOS PAL device process and applied it to a new family of 44-, 68-, and 84-pin 15-ns PLDs aimed at letting you meet your designs' speed and real estate targets.

In just a few short years, AMD has become a force in CMOS PLDs, building on our #1 spot in bipolar. With the new benefits that our breakthrough architecture CMOS family brings you, we continue moving towards the #1 spot in CMOS too.

By providing a breadth of architectures and technologies, we hope to make it easier for you to get your new product to market quickly enough to win in this ultra-competitive world.

Andy Robin
Director of Marketing
Programmable Logic

INTRODUCTION

This book introduces you to the new MACH 1 and MACH 2 families of programmable logic from Advanced Micro Devices. These devices provide programmable logic capabilities from around 900 gates to 3600 gates. Included in this book are a general discussion, the MACH110 and MACH210 final data sheets, the preliminary data sheets for the next three family members, and advance information on the final devices.

The general discussion deals with those issues that affect the entire device family, including a brief discussion of the PALASM® software used to configure the devices. Because of the common architecture, most of the understanding of the device can come from a look at the families as a whole. Individual devices differ only in number of resources.

The data sheets discuss items that are specific to the first four devices: the MACH110, MACH120, MACH130, and MACH210. They contain the basic DC and switching specifications. Other general specifications, such as switching waveforms and endurance, follow the data sheets, since they are the same for all devices.

Finally, an advance information sheet provides a look at the last member of the MACH 2 family: the MACH220.

The order in which the products appear in the databook has been changed in this edition. From this edition on, all devices will appear in numerical order according to the device name, regardless of release status. This should make it easier for you to find devices in future editions.

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MACH Device Family

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density, electrically-erasable CMOS PLD families**
- **900 to 3600 gate equivalents**
- **44 to 84 pins in cost-effective PLCC and CQFP packages**
- **32 to 128 macrocells**
- **0.8-µm CMOS provides predictable design-independent high speeds**
  - Commercial 15-ns/20-ns t_{PD}, 50-MHz/40-MHz f_{MAX}
  - Military 20-ns t_{PD}, 40-MHz f_{MAX}
- **PAL blocks connected by switch matrix**
  - Provides optimized global connectivity
  - Switch matrix integrates blocks into uniform device
- **Configurable macrocells**
  - Programmable polarity
  - Registered or combinatorial
  - Internal and I/O feedback
  - D-type or T-type flip-flops
  - Choice of clocks for each flip-flop
  - Input registers for MACH 2 family
- **Supported by popular industry-standard design software**
  - Schematic capture and text entry
  - Compilation and JEDEC file generation
  - Design simulation
  - Logic and timing models
- **Programmable on standard programmable logic device programmers**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	Gate Equivalents	Max Inputs	Max Outputs	Max Flip-Flops	Speed (ns)
MACH 1 Family							
MACH110	44	32	900	38	32	32	15, 20
MACH120	68	48	1200	56	48	48	15, 20
MACH130	84	64	1800	70	64	64	15, 20
MACH 2 Family							
MACH210	44	64	1800	38	32	64	15, 20
MACH220	68	96	2400	56	48	96	15, 20
MACH230	84	128	3600	70	64	128	15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced CMOS technology to offer a device with several times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

Their unique architecture makes these devices ideal for replacing large amounts of TTL logic. They are the first devices to provide such increased functionality without forcing the designer to sacrifice speed and cost.

The MACH devices consist of PAL blocks interconnected by a programmable switch matrix (figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into the PAL blocks. Designs that are not as modular can still be implemented since the switch matrix provides a high level of connectivity between the PAL blocks. This internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

The MACH family is supported by AMD's PALASM software development system. This software runs on PC/AT-compatible and 386-based systems. The package provides low-cost CAD capability while easing all the important phases of the designer's task: design entry, implementation, verification, programming, and

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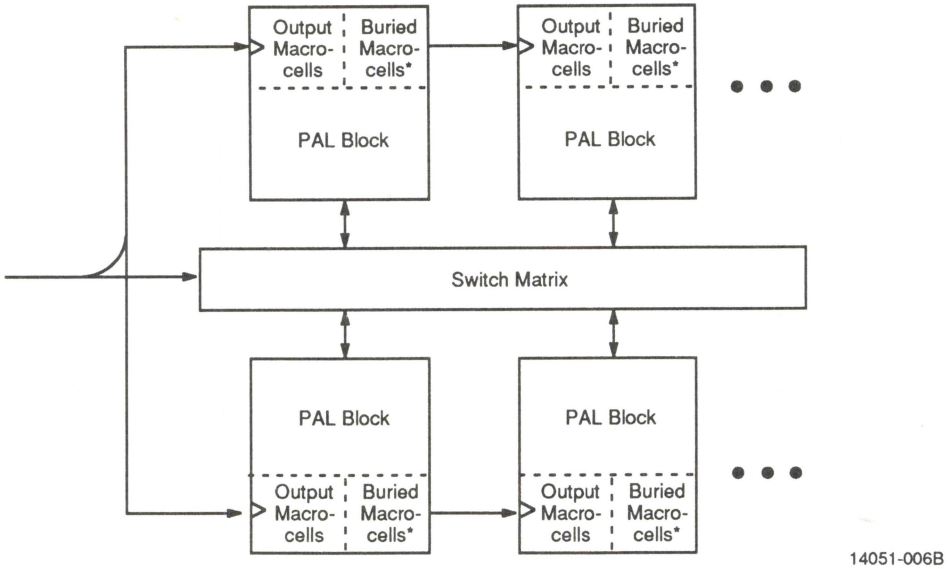
Issue Date: April 1991

testing. The MACH devices can be programmed on conventional PAL device programmers with appropriate personality and socket adapter modules.

The MACH 1 and MACH 2 families are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. The CMOS EE technology provides 100% testability, thus reducing the designer's prototype development costs.



* Buried macrocell available on MACH 2 devices only.

Figure 1. General MACH Device Block Diagram

THE MACH 1 AND MACH 2 FAMILIES

The MACH 1 and MACH 2 families each consist of several members. The first three members of each family are discussed in this book. The items that differentiate the members of the family are the number of pins, the number of macrocells, the amount of interconnect, and the number of clocks. The MACH 1 family has output macrocells; the MACH 2 family has output and buried macrocells. In all other respects, the two families are the same.

This provides a convenient way of migrating designs up or down with little difficulty. Because there is a choice of I/O-pin-to-macrocell ratio, the designer can choose a device that suits both his internal logic needs and his I/O needs. In the future, the software will also be able to provide automatic partitioning and device selection to make the design process device-independent.

The first devices range in pin count from 44 to 84, and in number of macrocells from 32 to 128. All devices are provided in cost-effective PLCC packages; military versions are available in CQFP packages.

Design Methodology

An important aspect of the MACH family is the fact that design tools are widely available both from AMD and from third-party software vendors. AMD provides PALASM software as a lower cost baseline tool set and works with tools vendors to ensure broad MACH device support. This allows designers to do MACH device designs using the same tools that they would use to do PAL device designs, whether PALASM software or any of the other popular PAL device design packages.

Design entry is the same as that used for PAL devices, including the capability of using schematic capture for design packages such as PALASM 4 software. The basic logic processing steps are also the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all the packages, and other options for simulating the timing and board-level behavior of the MACH devices are available as options. In all cases, the desired end result is a JEDEC file that can be downloaded to a programmer for device configuration.

The MACH design methodology differs from that of a PAL device somewhat due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture,

state machine equations, or Boolean equations—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the fitter will vary from design to design, but 70% utilization is typical.

In general, letting the software decide the best fit and pin placement automatically for the first iteration of the design provides the best chance of fitting. It can also be useful to implement large designs incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. However, it is possible to pre-place signals. If done carefully, this can help the software fit difficult designs; if not done carefully, it may make it harder for the design to fit. Guidelines on specifying the initial pinout are provided in the MACH user's manual.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. If changes are too dramatic, then it may be necessary to refit the design, potentially resulting in a new pinout. The stability of the design and the expected extent of any changes should therefore be considered before committing the design to layout. Careful designs that target about 70% utilization will make future changes much easier. Hints on designing for change can be found in the software documentation.

In all cases, the way the design is partitioned and placed into the MACH device by the software does not affect the performance of the design. With designs that do not fit, it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or using multi-level logic), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Functional Description

The fundamental architecture of the MACH devices consists of several PAL blocks interconnected by a switch matrix. The switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together the PAL blocks and switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, outputs, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes used. Because of the use of programmable interconnections, the product-term arrays have been decoupled from the switch matrix, the macrocells, and the I/O pins. This provides much greater flexibility, and allows designs to be placed and routed efficiently and quickly.

The internal architecture is such that all signals incur the same delays, regardless of routing. This means that the performance of a design is design-independent, and is known before the design is even begun.

The PAL Blocks

The PAL blocks can be viewed as independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. The PAL blocks communicate with each other only through the switch matrix.

Each PAL block contains a product-term array, a logic allocator, macrocells, and I/O cells. The product-term array generates the basic logic, although the number of product terms per macrocell is variable. The logic allocator distributes the product terms to the macrocells. This allows the distribution of product terms as required by the design. The macrocell configures the signal, and the I/O cell delivers the final signal to the output pin.

Each PAL block additionally contains an asynchronous reset product term and an asynchronous preset product term. This allows the flip-flops within a single PAL block to be initialized as a bank. There are also several three-state product terms that provide three-state control to the I/O cells.

The Switch Matrix

The switch matrix takes all dedicated inputs, I/O feedback signals, and buried feedback signals and routes them as needed to the various PAL blocks. Feedback signals that only return to the same PAL block still go through the switch matrix. This provides a way for the PAL blocks to communicate with each other with consistent, predictable delays. It is the switch matrix which makes the MACH devices more than just multiple PAL devices on a single chip.

For designs that consist of smaller functional units that are connected together, the PAL blocks provide the routing software with local full connectivity for each unit, connected by the switch matrix. For designs that are larger in scope, the switch matrix allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into the PAL blocks through the switch matrix so that the designer does not have to be concerned with the internal organization.

The Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the switch matrix, and are provided in both true and complement forms for efficient logic implementation.

Because the number of product terms allocated to each macrocell is not fixed, the full sum of products is not realized in the array. The product terms drive the logic

allocator, which allocates the product terms to the appropriate macrocells.

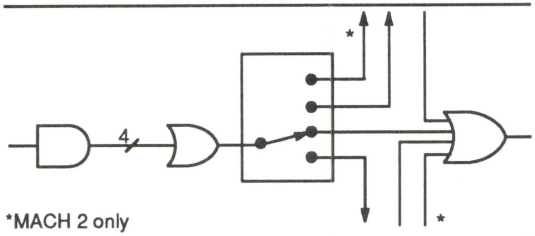


Figure 2. The Logic Allocator

The Logic Allocator

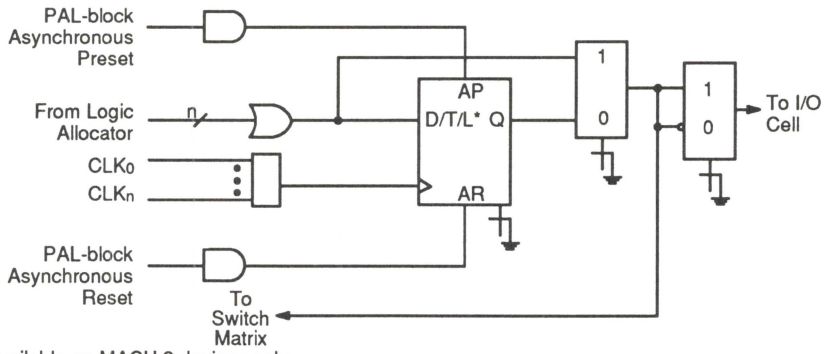
The logic allocator (figure 2) is a block within which different product terms are allocated to the appropriate macrocells in blocks of four product terms. The availability and distribution of product terms is automatically considered by the software as it places and routes functions within the PAL block. The product-term distribution has been designed to provide high utilization of product terms. Complex functions using many product terms are possible, yet fewer product terms will be left unused—or wasted—when the design is complete.

The Macrocell

There are two fundamental types of macrocell: the output macrocell and the buried macrocell. The buried macrocell is only found in MACH 2 devices. The use of buried macrocells effectively doubles the number of macrocells available without increasing the pin count.

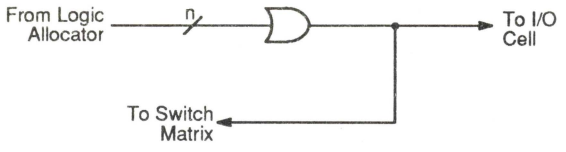
Both macrocell types can generate registered or combinatorial outputs. For the MACH 2 series, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Programmable polarity (for output macrocells) and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

The output macrocell (figure 3) sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in figure 4.

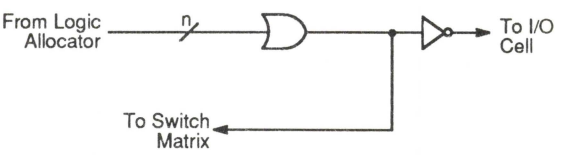


* Latch option available on MACH 2 devices only.

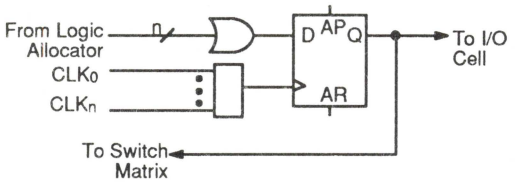
Figure 3. Output Macrocell



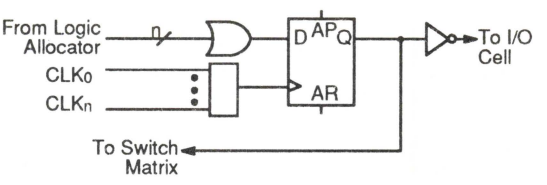
a. Combinatorial, Active High



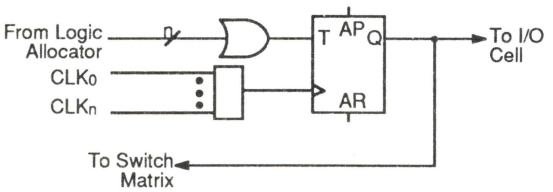
b. Combinatorial, Active Low



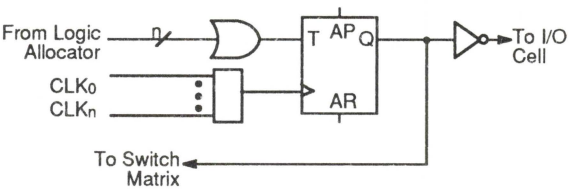
c. D-type Register, Active High



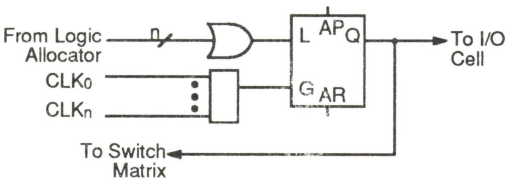
d. D-type Register, Active Low



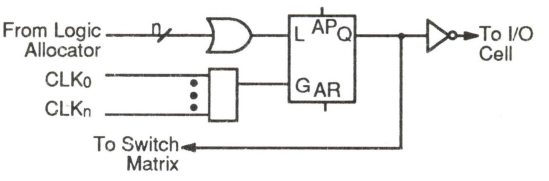
e. T-type Register, Active High



f. T-type Register, Active Low



g. Latch, Active High (MACH 2 only)



h. Latch, Active Low (MACH 2 only)

14051-002B

Figure 4. Output Macrocell Configurations

The buried macrocell (figure 4) does not send its output to an I/O cell. The output of a buried macrocell is provided only as an internal feedback signal which feeds the switch matrix. This allows the designer to generate additional logic without requiring additional pins.

In addition to the capabilities of the output macrocell, the buried macrocell allows the use of registered or latched inputs. The input register is a D-type flip-flop; the input latch is a transparent-low D-type latch. Once configured as a registered or latched input, the buried macrocell cannot generate logic from the product-term array. The basic buried macrocell configurations are shown in figure 5.

The flip-flops in either macrocell type can be clocked by one of several clock pins. Registers are clocked on the rising edge of the clock input. Latches hold their data when the gate input is HIGH. Clock pins are also available as inputs, although care must be taken when a signal acts as both clock and input to the same device. All flip-flops have asynchronous reset and preset. This is controlled by the common product terms that control all flip-flops within a PAL block. For a single PAL block, all flip-flops, whether in an output or a buried macrocell, are initialized together.

The I/O Cell

The I/O cell (figure 6) provides a three-state output buffer. The three-state buffer can be left permanently enabled, for use only as an output; permanently disabled, for use as an input; or it can be controlled by one of two product terms, for bidirectional signals and bus connections. The two product terms provided are common to a bank of I/O cells.

Register Preload

All registers on the MACH devices can be preloaded from the I/O pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Observability

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH devices offer an observability feature that allows the user to send hidden buried register values to observable output pins.

For macrocells that are configured as combinatorial, the observability function suppresses the selection of the combinatorial output by forcing the macrocell output multiplexer into registered output mode. The observability function allows observation of the associated registers by overriding the output enable control and enabling the output buffer.

Power-up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. The actual values of the outputs of the MACH devices will depend on the configuration of the macrocell. The V_{CC} rise must be monotonic and the reset delay time is 10 µs maximum.

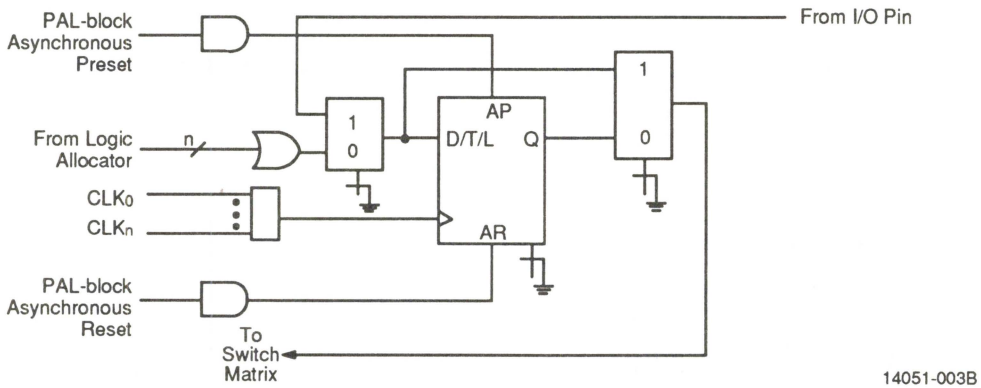


Figure 5. Buried Macrocell (MACH 2 only)

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit, but test vectors containing preload can be used independently of the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Programming and Erasing

The MACH devices can be programmed on standard logic programmers. They may also be erased to reprogram a previously configured device with a new program. Erasure is automatically performed by the programming hardware. No special erase operation is required.

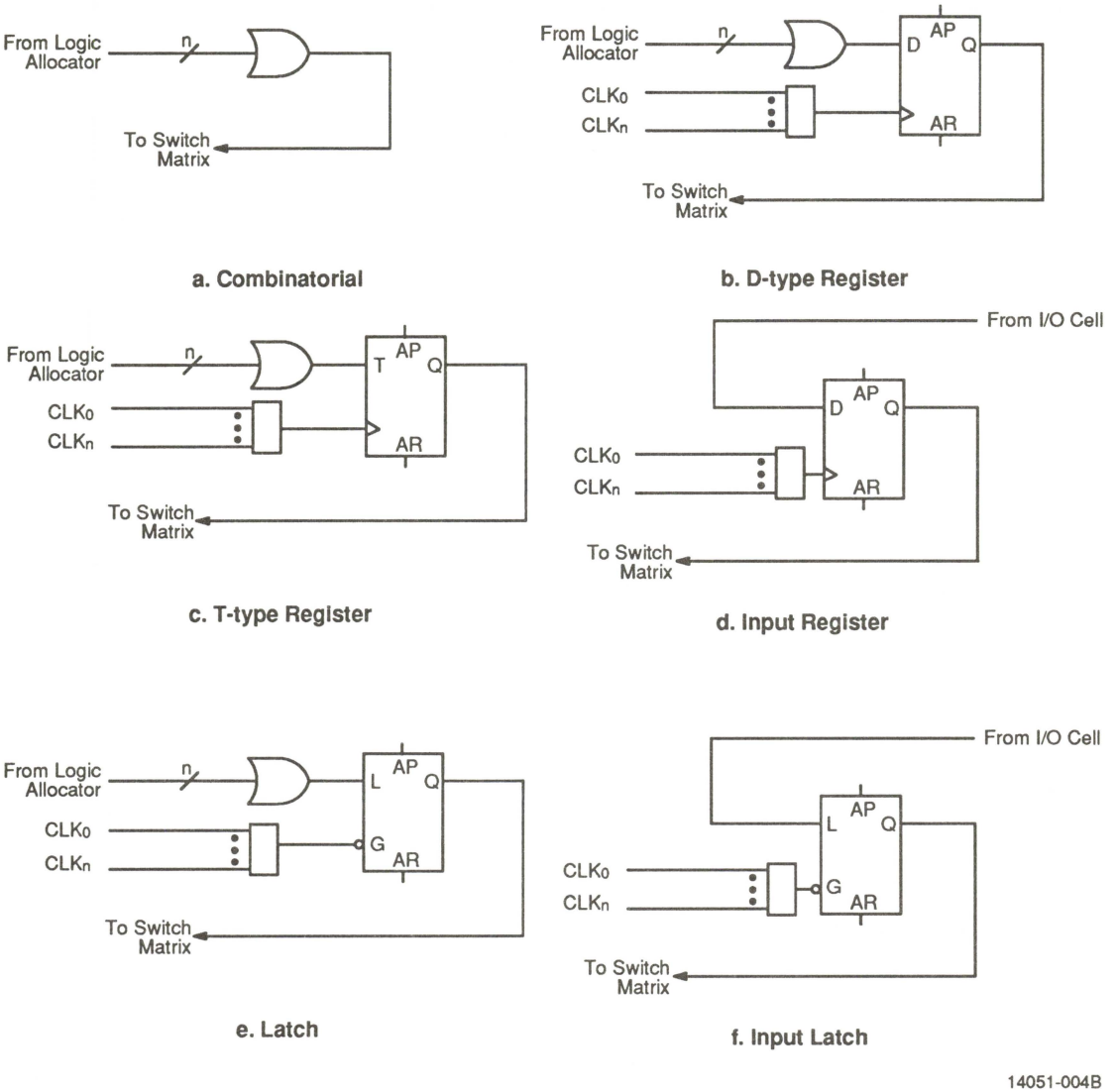


Figure 6. Buried Macrocell Configurations (MACH 2 only)

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.8-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals.

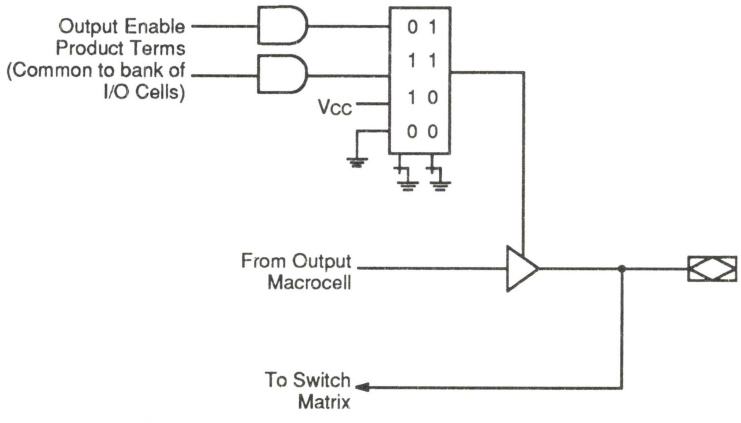


Figure 7. I/O Cell

MACH110-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 38 Inputs
- 32 Outputs
- 32 Flip-Flops
- 2 "PAL22V16" Blocks
- Pin-compatible with MACH210

GENERAL DESCRIPTION

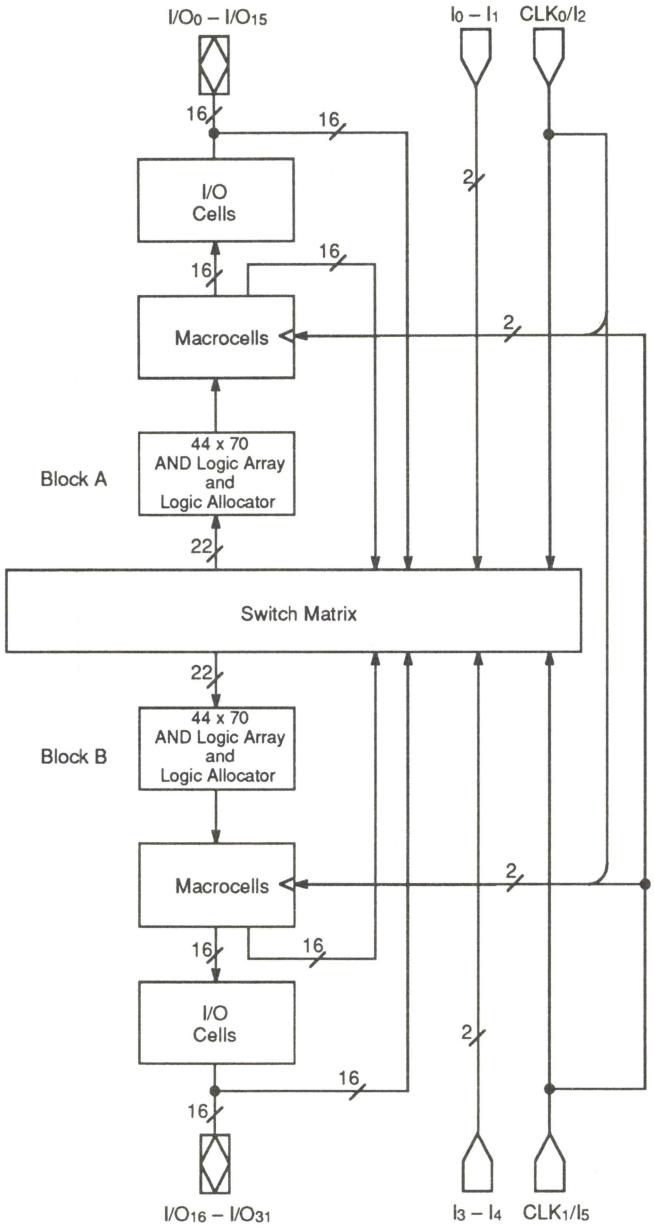
The MACH110 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH110 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH110 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication# 14127 Rev. C Amendment/0
Issue Date: April 1991

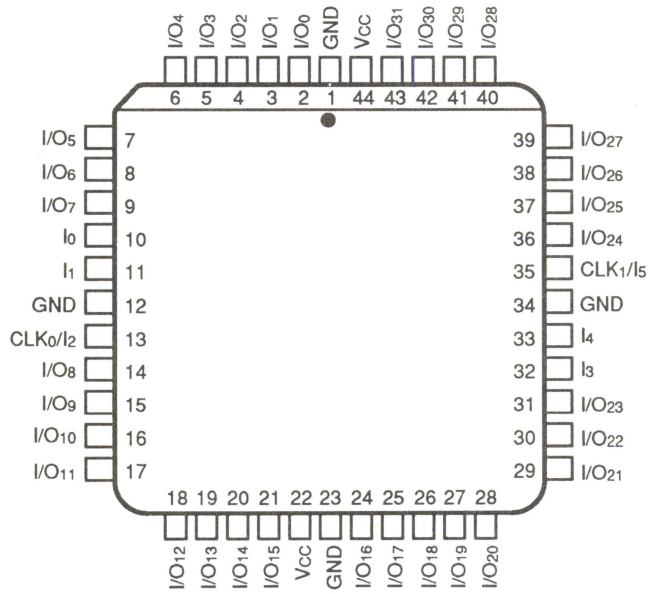
BLOCK DIAGRAM



14127-001B

CONNECTION DIAGRAM
Top View

PLCC/CQFP



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
VCC	Supply Voltage

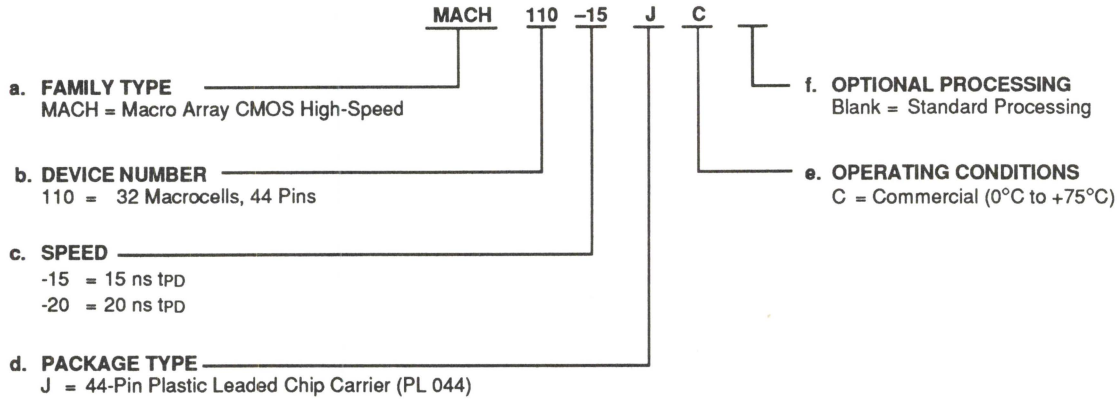
14127-002A

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. Family Type
b. Device Number
c. Speed
d. Package Type
e. Operating Conditions
f. Optional Processing



Valid Combinations
MACH110-15JC
MACH110-20JC

Valid Combinations

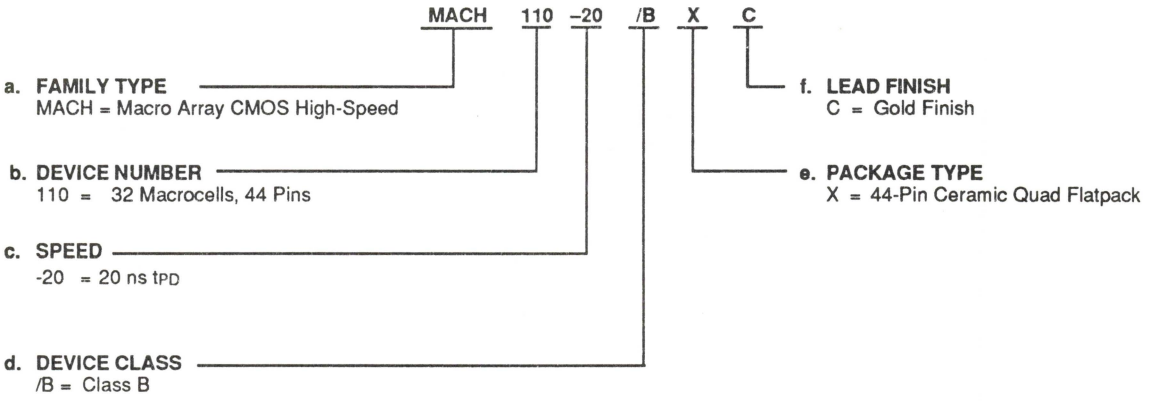
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION (Preliminary)

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Device Number**
c. **Speed**
d. **Device Class**
e. **Package Type**
f. **Lead Finish**



Valid Combinations
MACH110-20/BXC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH110 consists of two PAL blocks connected by a switch matrix. There are 32 I/O pins and 6 dedicated input pins feeding the switch matrix. These signals are distributed to the two PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH110 (figure 8) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the three-state product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH110 switch matrix is fed by the 6 dedicated inputs and all of the feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH110 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the three-state product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH110 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

The Macrocell

The MACH110 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH110 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

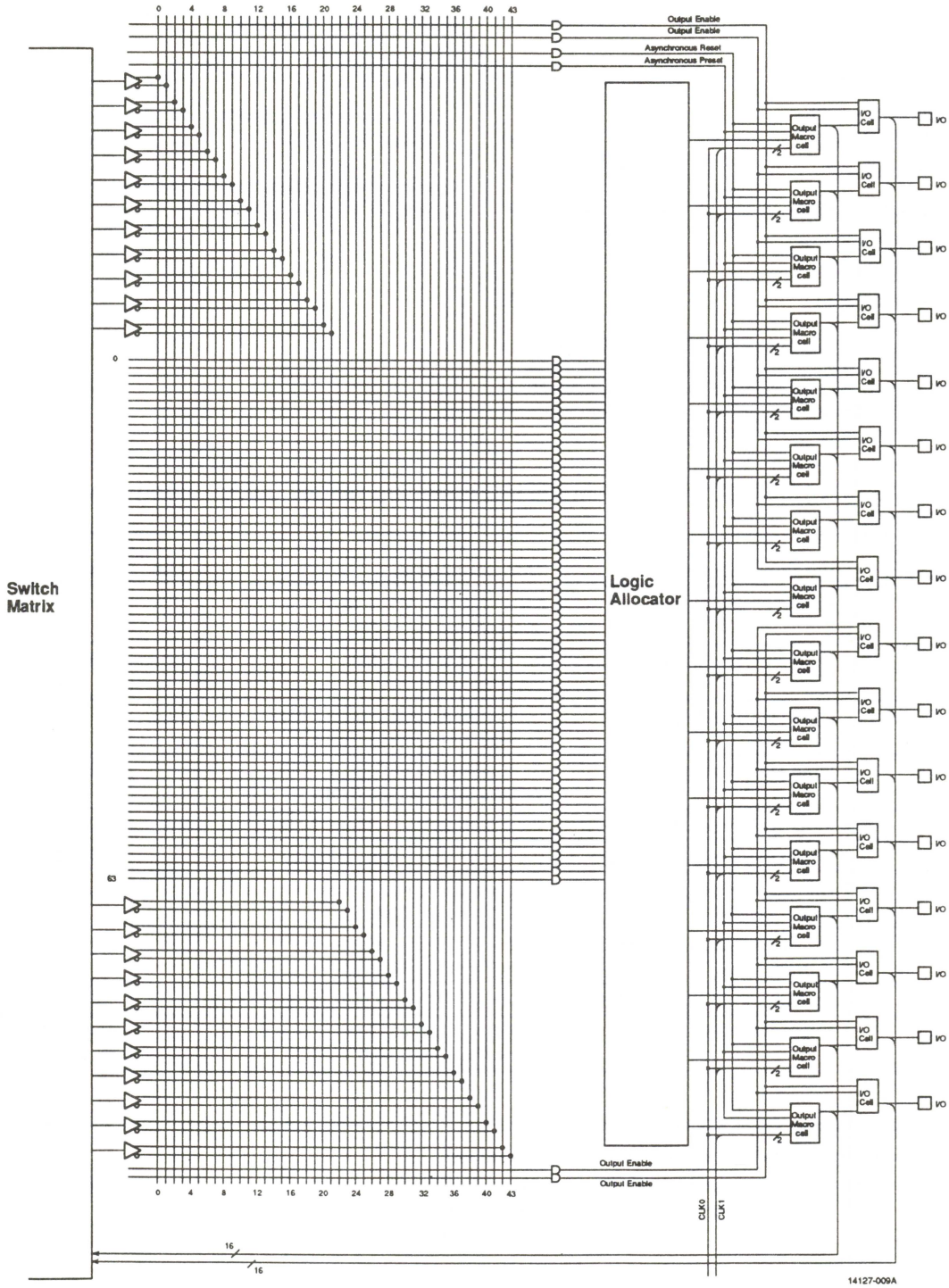


Figure 8. MACH110 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		150	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min.	Max.	Min.	Max.	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	12		15		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	45.5		37		MHz
		Internal Feedback		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					15		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		200	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

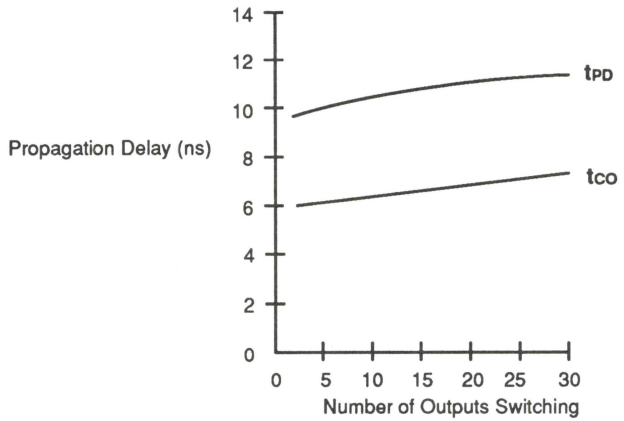
PRELIMINARY							
Parameter Symbol	Parameter Description				-20		Unit
					Min.	Max.	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t_S + t_{CO})	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	1/(t_{WL} + t_{WH})		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{AP}	Asynchronous Preset to Registered Output					25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				20		ns
t_{APR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

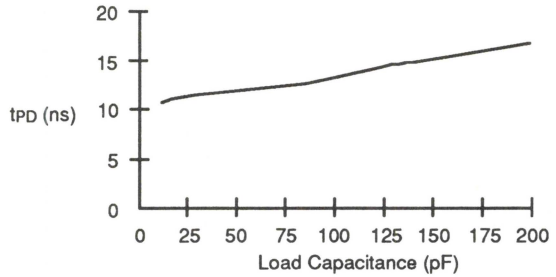
TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



t_{PD}, t_{CO} vs Number of Outputs Switching

14127-005A

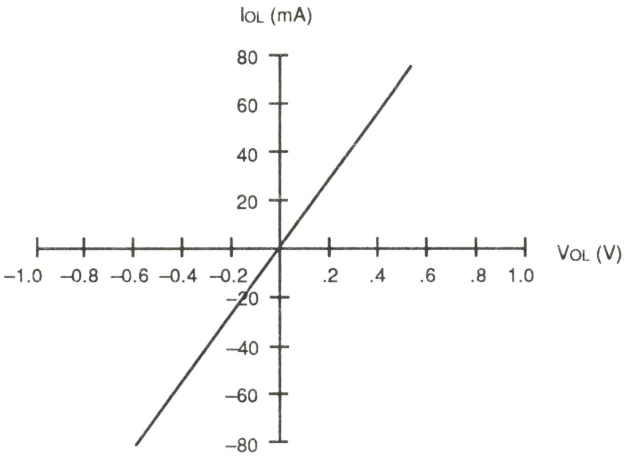


14127-006A

t_{PD} vs Load Capacitance

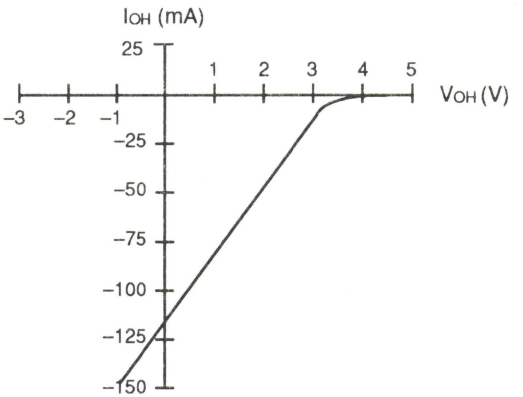
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



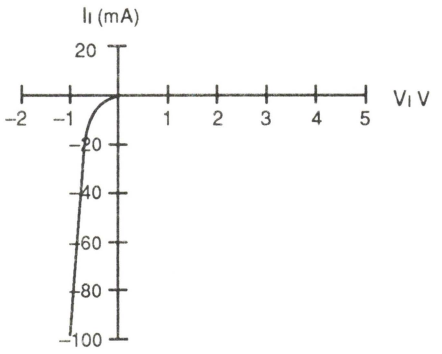
Output, LOW

14127-007A



Output, HIGH

14127-008A

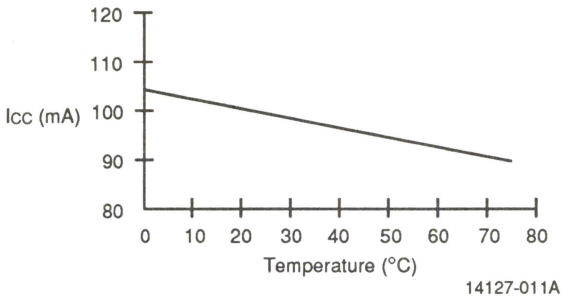


14127-009A

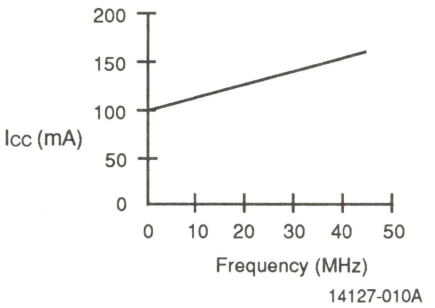
Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C, frequency = 0 MHz unless otherwise specified



I_{CC} vs. Operating Temperature



I_{CC} vs. Operating Frequency

MACH120-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 48 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 56 Inputs
- 48 Outputs
- 48 Flip-flops
- 4 PAL blocks
- Pin-compatible with MACH220

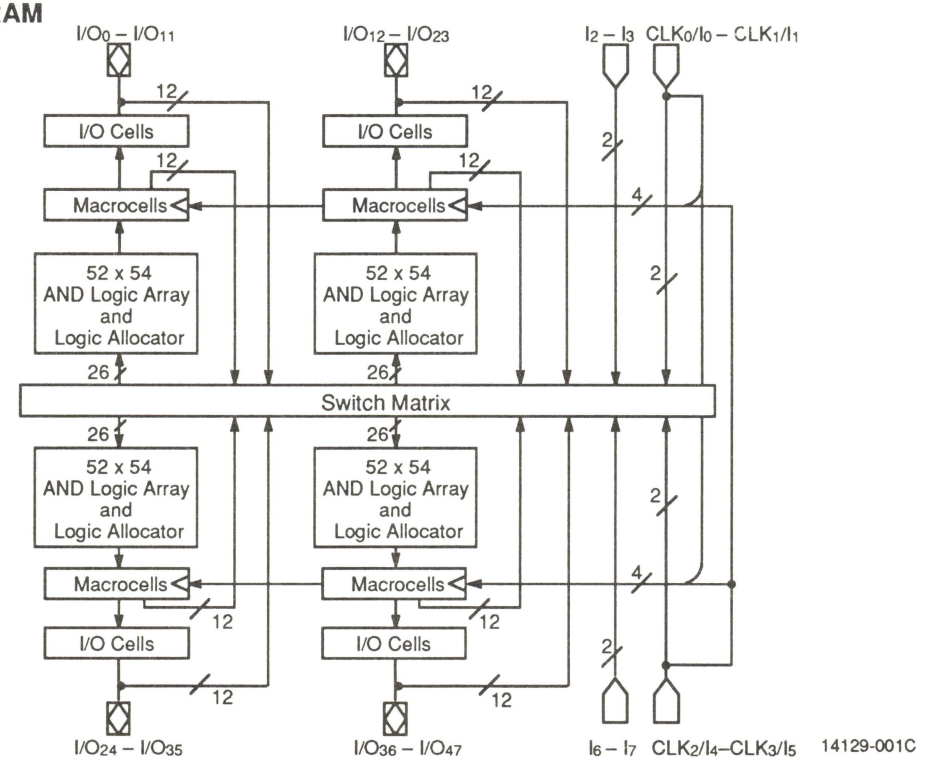
GENERAL DESCRIPTION

The MACH120 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately five times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH120 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

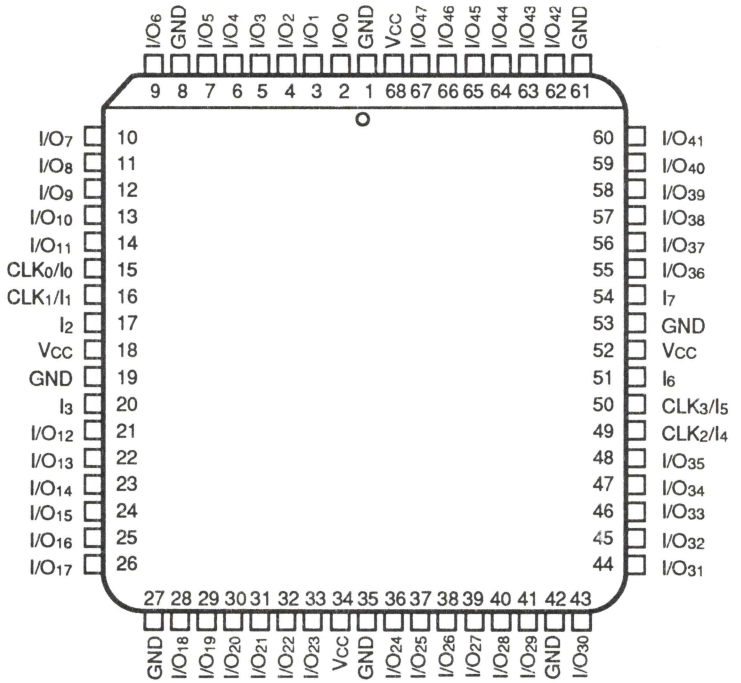
The MACH120 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

BLOCK DIAGRAM



CONNECTION DIAGRAMS

Top View



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
Vcc	Supply Voltage

FUNCTIONAL DESCRIPTION

The MACH120 consists of four PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH120 (figure 9) contains a 48-product-term logic array, a logic allocator, 12 macrocells and 12 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 12 I/O cells are divided into 2 banks of 6 macrocells. Each bank is allocated two of the three-state product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH120 switch matrix is fed by the 8 dedicated inputs and all of the feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 12 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH120 product-term array consists of 48 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the three-state product terms are used for the first six I/O cells; the other two control the last six macrocells.

The Logic Allocator

The logic allocator in the MACH120 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

The Macrocell

The MACH120 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH120 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to six I/O cells.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

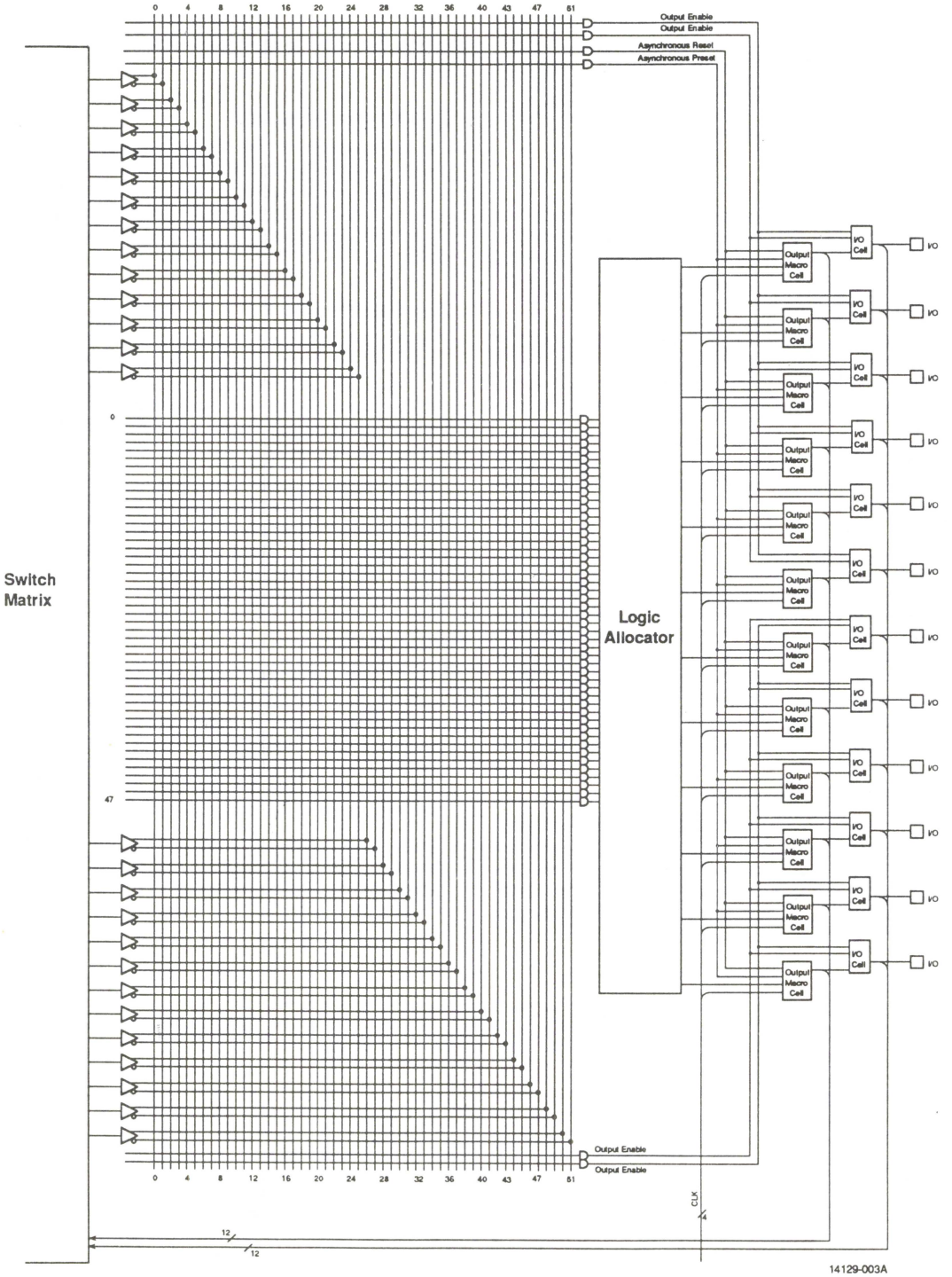


Figure 9. MACH120 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz		pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description				-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10			13	ns
				T-type	12		15		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(ts + tco)	D-type	50		40		MHz
				T-type	45.5		37		MHz
		Internal Feedback		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	1/(twL + twH)		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					15		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions.
3. Parameters measured with 24 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

MACH130-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 70 Inputs
- 64 Outputs
- 64 Flip-flops
- 4 "PAL26V16" Blocks with buried Macrocells
- Pin-compatible with MACH230

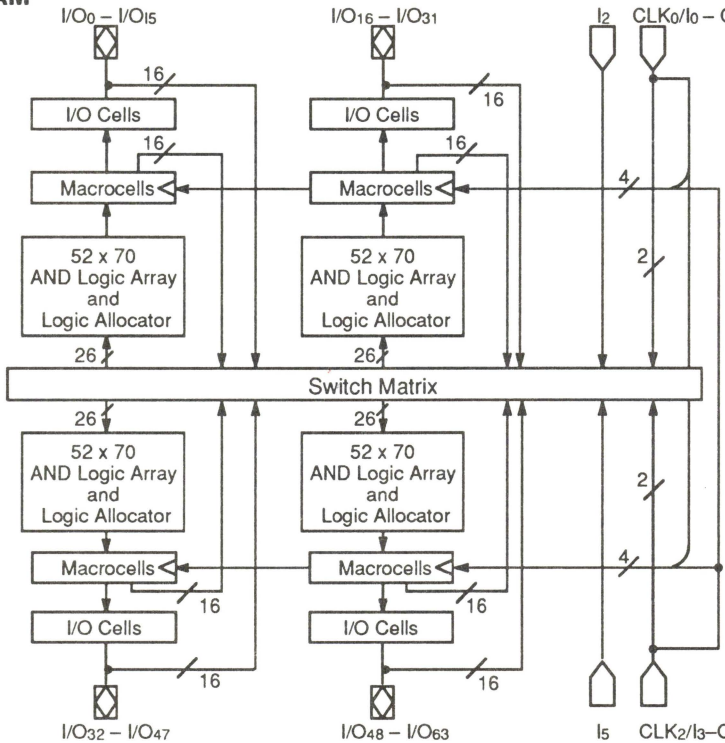
GENERAL DESCRIPTION

The MACH130 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH130 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

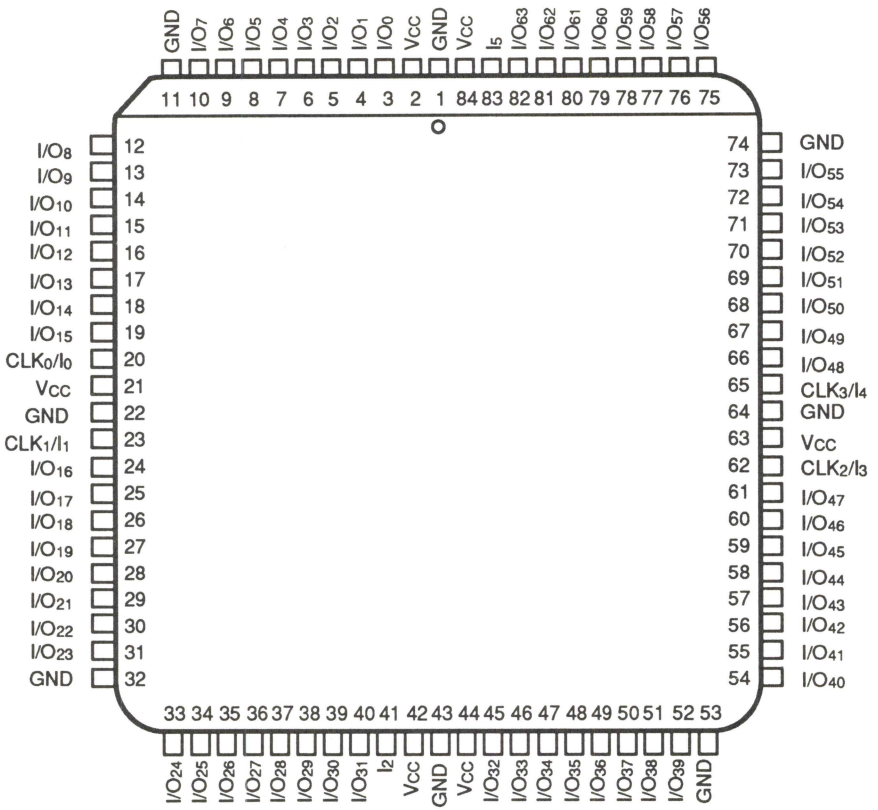
The MACH130 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View

PLCC/CQFP



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
VCC	Supply Voltage

FUNCTIONAL DESCRIPTION

The MACH130 consists of four PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH130 (figure 10) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the three-state product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH130 switch matrix is fed by the 6 dedicated inputs and all of the feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH130 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the three-state product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH130 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

The Macrocell

The MACH130 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH130 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

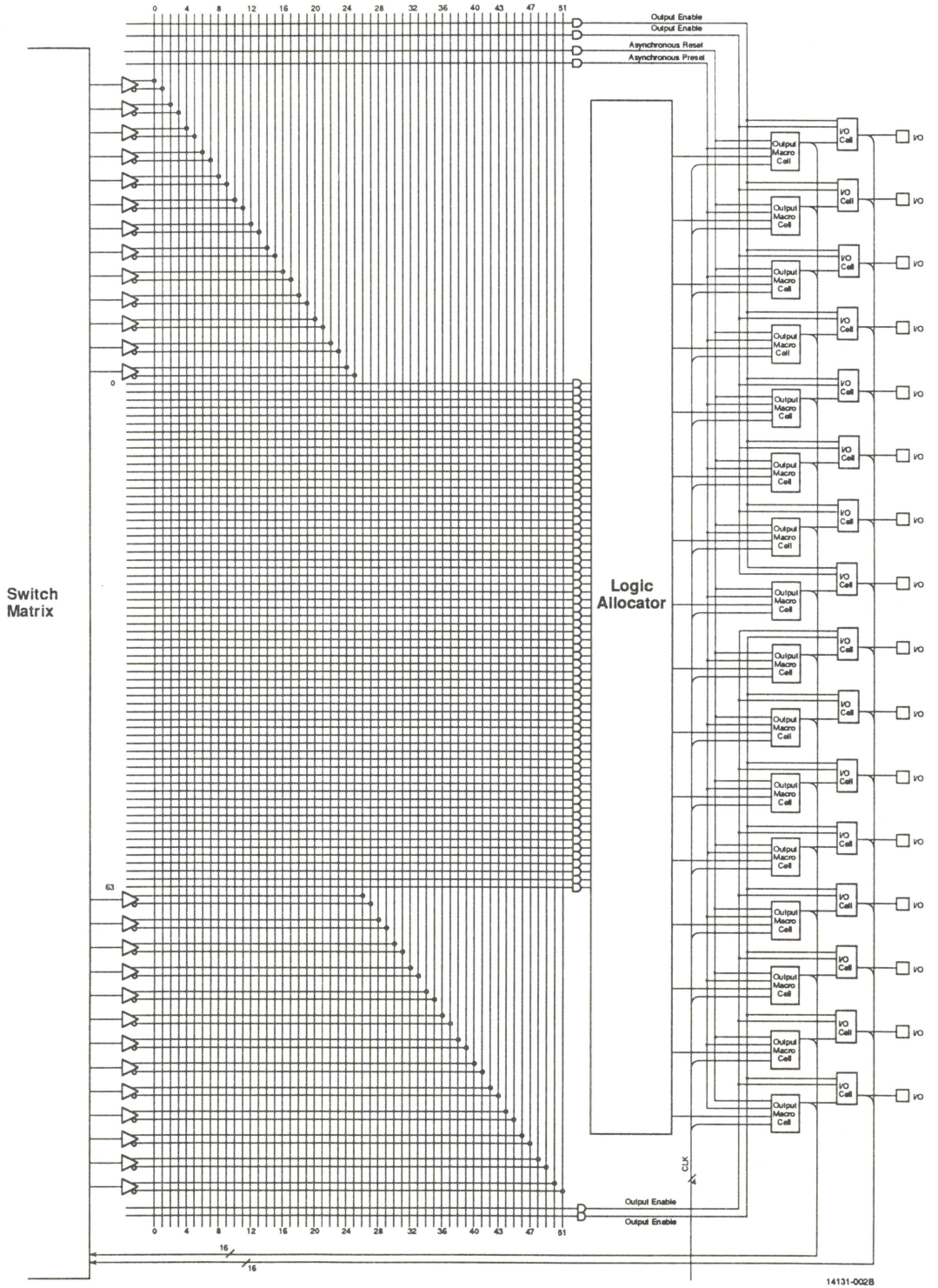


Figure 10. MACH130 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz		pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description				-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10			13	ns
				T-type	12		15		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t_S + t_{CO})	D-type	50		40		MHz
				T-type	45.5		37		MHz
		Internal Feedback		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	1/(t_{WL} + t_{WH})		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					15		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		220	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz		pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

PRELIMINARY							
Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{AP}	Asynchronous Preset to Registered Output					25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				20		ns
t_{APR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

MACH210-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 64 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 38 Inputs
- 32 Outputs
- 64 Flip-flops
- 4 "PAL22V16" blocks with buried macrocells
- Pin-compatible with MACH110

GENERAL DESCRIPTION

The MACH210 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

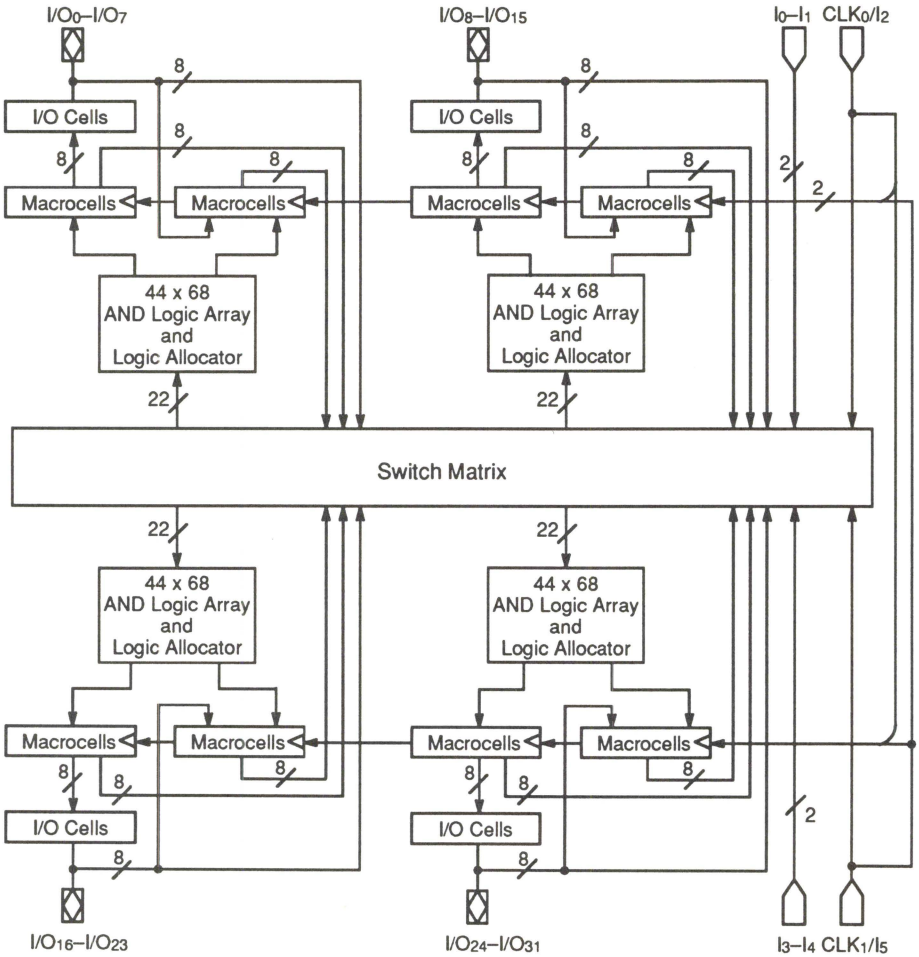
The MACH210 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH210 has two kinds of macrocell: output and buried. The MACH210 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH210 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

Publication# 14128 Rev. C Amendment/0
Issue Date: April 1991

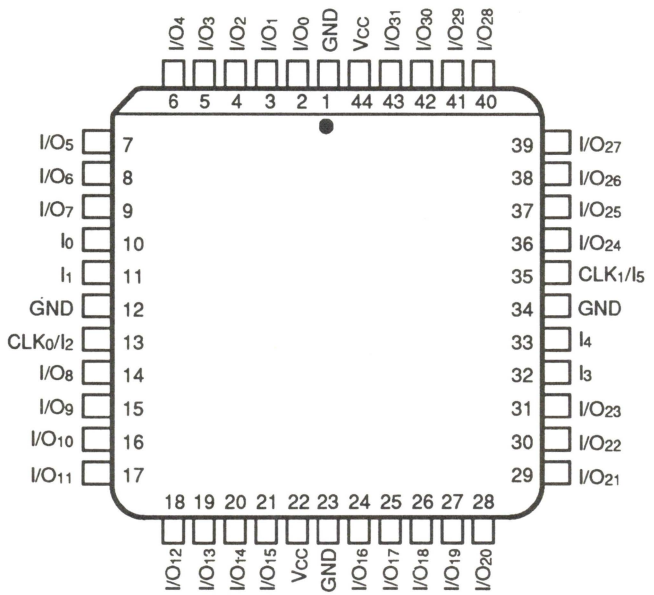
BLOCK DIAGRAM



14128-001B

CONNECTION DIAGRAM
Top View

PLCC/CQFP



14127-002A

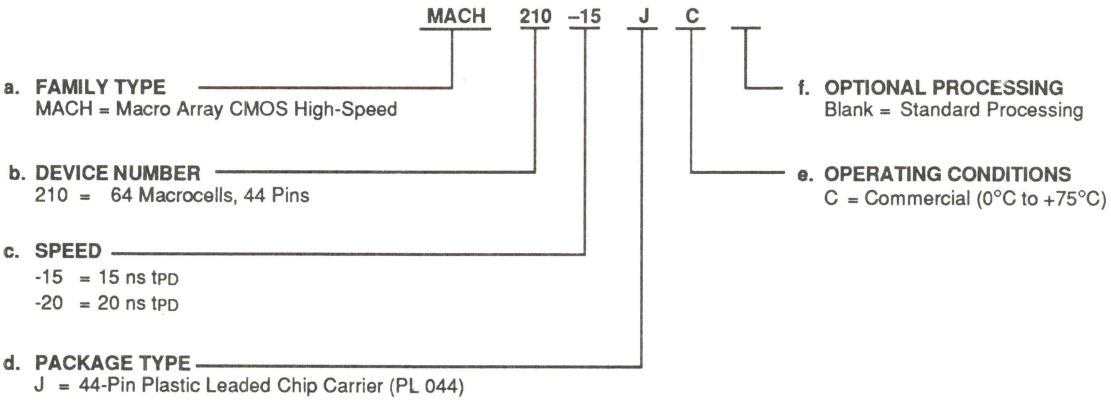
Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
Vcc	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Device Number**
c. **Speed**
d. **Package Type**
e. **Operating Conditions**
f. **Optional Processing**



Valid Combinations
MACH210-15JC
MACH210-20JC

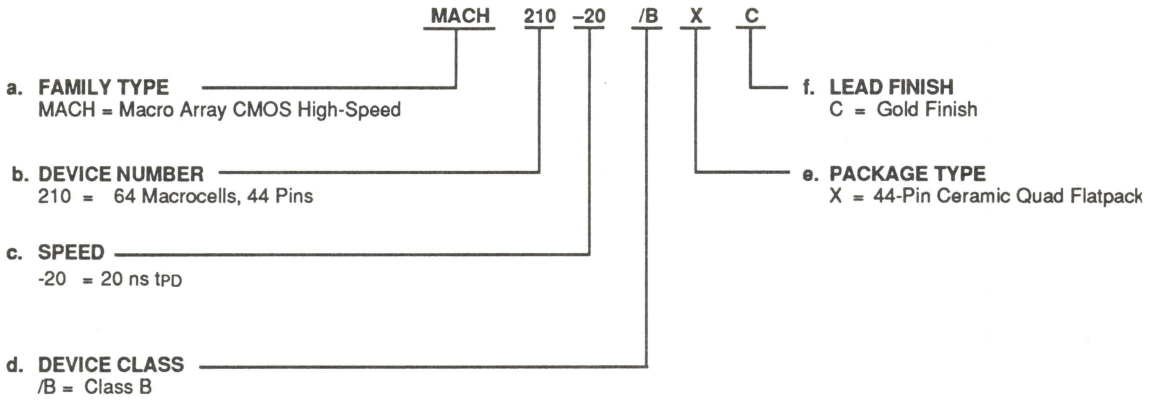
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION (Preliminary)
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Device Number**
c. **Speed**
d. **Device Class**
e. **Package Type**
f. **Lead Finish**



Valid Combinations
MACH210-20/BXC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH210 consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs. This device provides two kinds of macrocell: output macrocells and buried macrocells. This adds greater logic density without affecting the number of pins.

The PAL Blocks

Each PAL block in the MACH210 (figure 11) contains a 64-product-term logic array, a logic allocater, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two three-state product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH210 switch matrix is fed by the 6 dedicated inputs and all of the feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH210 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH210 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

The Macrocell

The MACH210 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH210 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

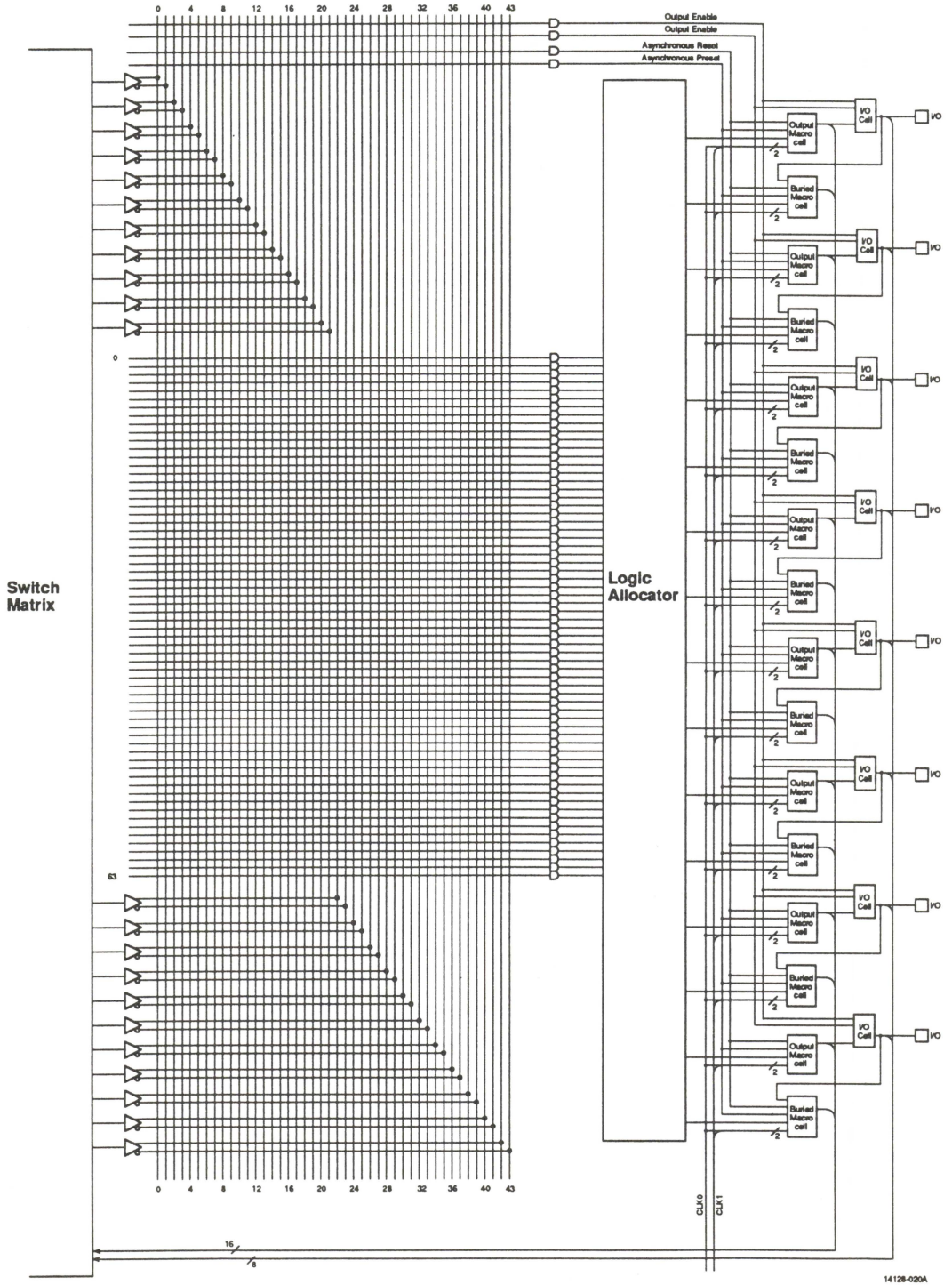


Figure 11. MACH210 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f =0 MHz		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min.	Max.	Min.	Max.	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	12		15		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(ts + tco)	D-type	50		40		MHz
				T-type	45.5		37		MHz
		Internal Feedback		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	1/(t_{WL} + t_{WH})		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		13		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)				10		12		ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					17		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		ns
				T-type	14		17		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	1/(t_{WICL} + t_{WICH})			83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				12		15		ns
t_{WIGZ}	Input Latch Gate Width LOW				6		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)(Cont'd)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min.	Max.	Min.	Max.	
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	10		15		ns
t_{AP}	Asynchronous Preset to Registered Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)		15		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		220	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Register Data Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t_S + t_{CO})	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	1/(t_{WL} + t_{WH})		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate						ns
t_{HL}	Latch Data Hold Time						ns
t_{GO}	Gate to Output (Note 3)						ns
t_{GWL}	Gate Width LOW						ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch						ns
t_{SIR}	Input Register Setup Time						ns
t_{HIR}	Input Register Hold Time						ns
t_{ICO}	Input Register Clock to Combinatorial Output						ns
t_{ICS}	Input Register Clock to Output Register Setup						ns
t_{WICL}	Input Register			LOW			ns
t_{WICH}	Clock Width			HIGH			ns
f_{MAXIR}	Maximum Input Register Frequency (Note 4)		1/(t_{WICL} + t_{WICH})				MHz
t_{SIL}	Input Latch Setup Time						ns
t_{HIL}	Input Latch Hold Time						ns
t_{IGO}	Input Latch Gate to Combinatorial Output						ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch						ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate						ns
t_{IGS}	Input Latch Gate to Output Latch Setup						ns

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2) (Cont'd)

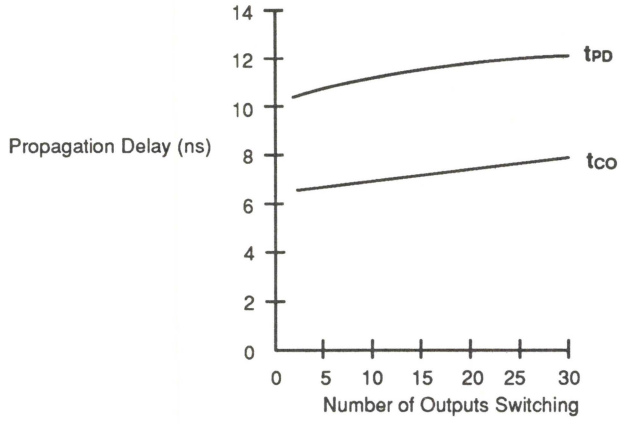
Parameter Symbol	Parameter Description	-20		Unit
		Min.	Max.	
t_{WIGZ}	Input, Latch Gate Width LOW	ns		
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			ns
t_{AR}	Asynchronous Reset to Registered Output	25	ns	
t_{ARW}	Asynchronous Reset Width (Note 4)		ns	
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)		ns	
t_{AP}	Asynchronous Preset to Registered Output	25	ns	
t_{APW}	Asynchronous Preset Width (Note 4)		ns	
t_{APR}	Asynchronous Preset Recovery Time (Note 4)		ns	
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

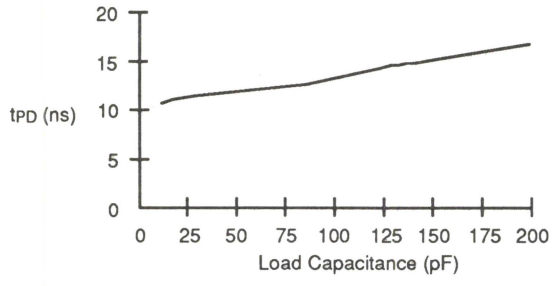
TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



t_{PD}, t_{CO} vs Number of Outputs Switching

14127-005A

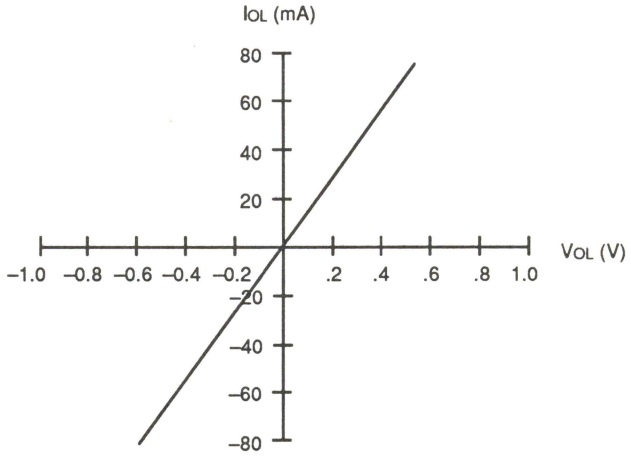


t_{PD} vs Load Capacitance

14127-006A

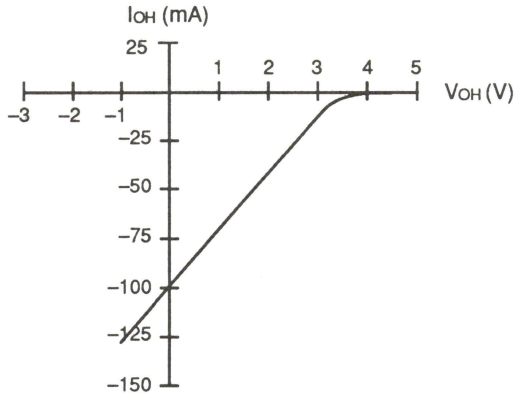
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



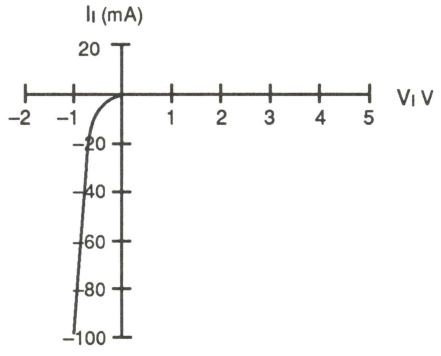
Output, LOW

14127-007A



Output, HIGH

14127-008A

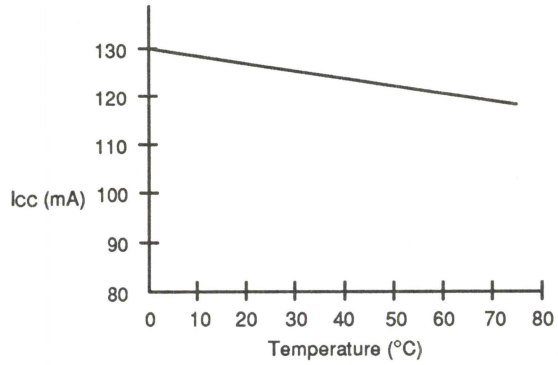


14127-009A

Input

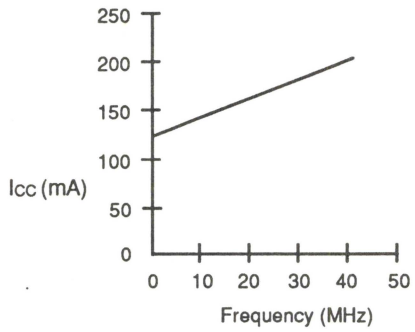
TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C, frequency = 0 MHz unless otherwise specified



14127-011A

I_{CC} vs. Operating Temperature



14127-010A

I_{CC} vs. Operating Frequency

MACH220-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 96 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 56 Inputs
- 48 Outputs
- 96 Flip-flops
- 8 PAL blocks with buried macrocells
- Pin-compatible with MACH120

GENERAL DESCRIPTION

The MACH220 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately nine times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

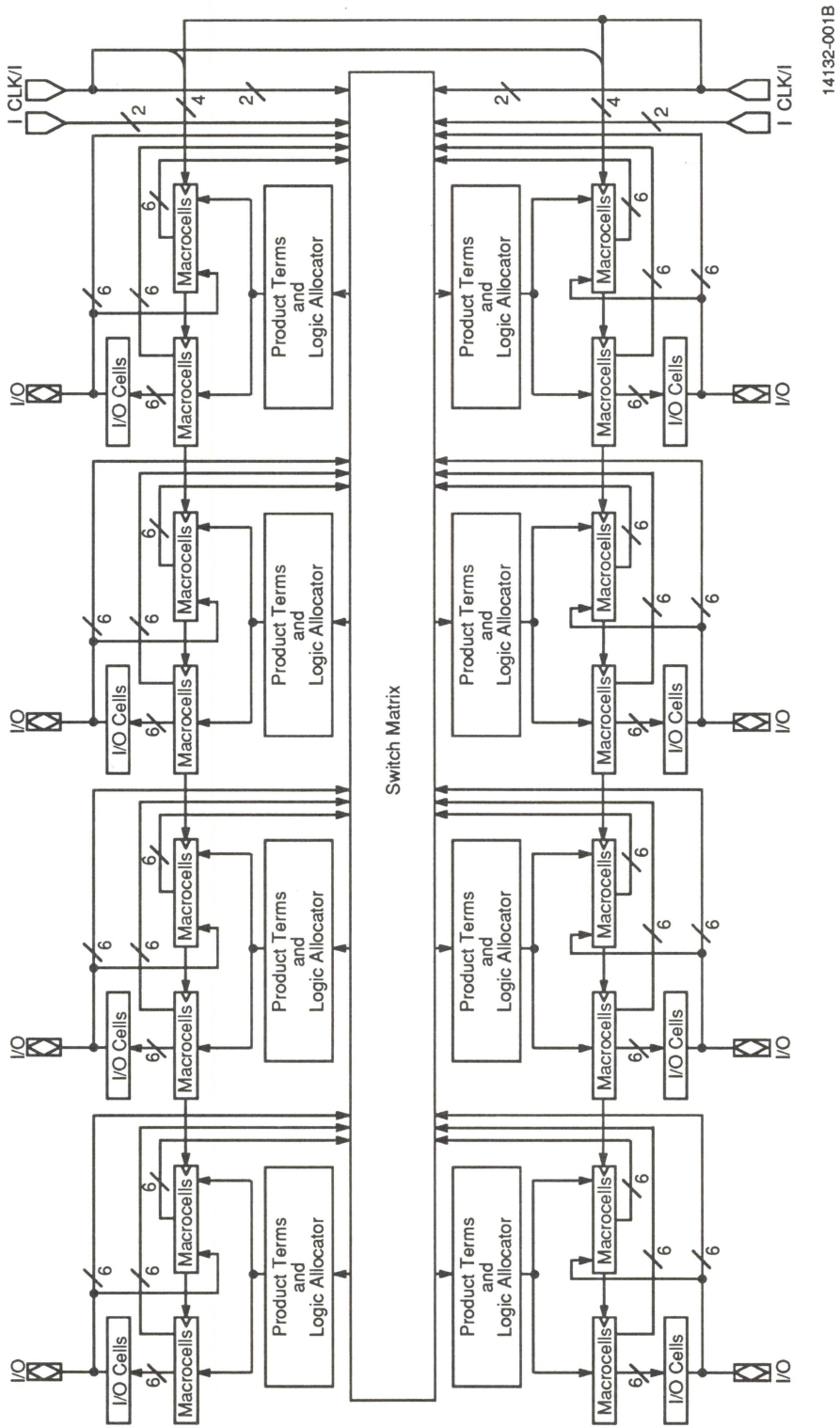
The MACH220 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH220 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH220 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Publication # 14130 Rev. C Amendment/0
Issue Date: April 1991

BLOCK DIAGRAM



MACH230-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 128 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 70 Inputs
- 64 Outputs
- 128 Flip-flops
- 8 "PAL26V16" blocks with buried macrocells
- Pin-compatible with MACH130

GENERAL DESCRIPTION

The MACH230 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately twelve times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

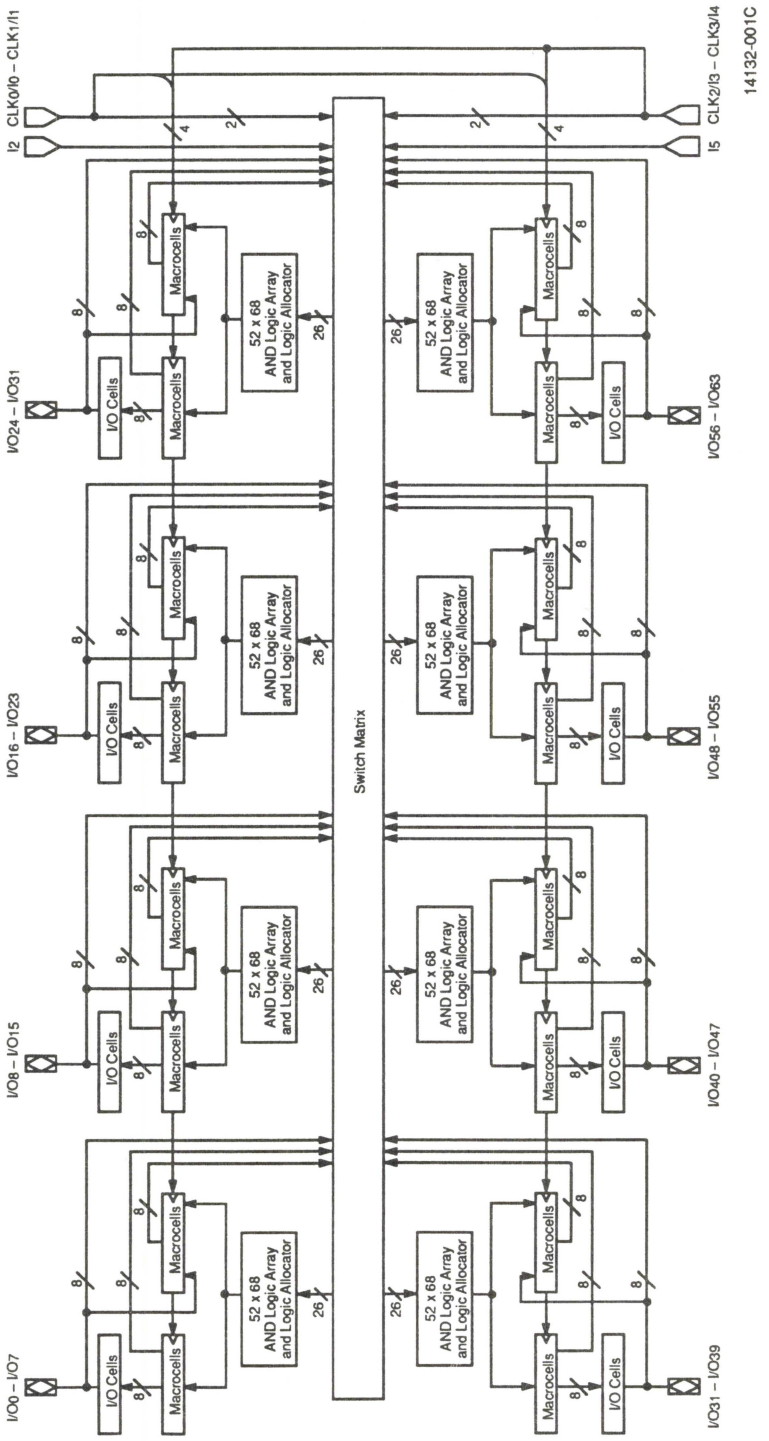
The MACH230 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH230 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH230 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

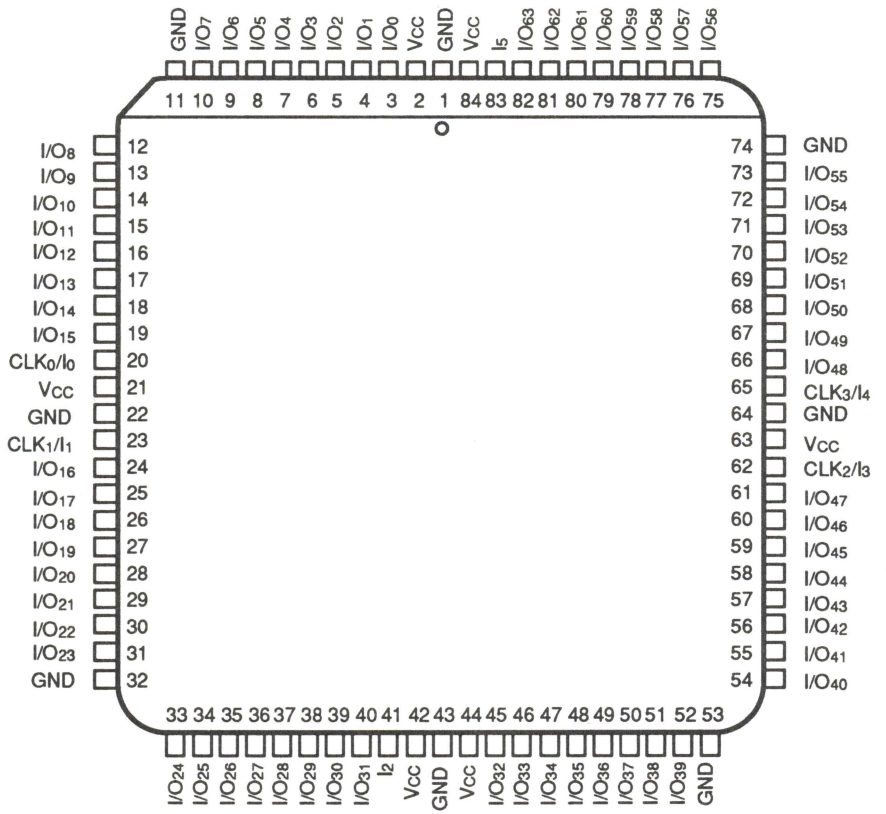
Publication # 14132 Rev. C Amendment/0
Issue Date: April 1991

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View

PLCC/CQFP



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
VCC	Supply Voltage

FUNCTIONAL DESCRIPTION

The MACH230 consists of eight PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH230 (figure 12) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two three-state product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH230 switch matrix is fed by the 6 dedicated inputs and all of the feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH230 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH230 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

The Macrocell

The MACH230 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH230 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

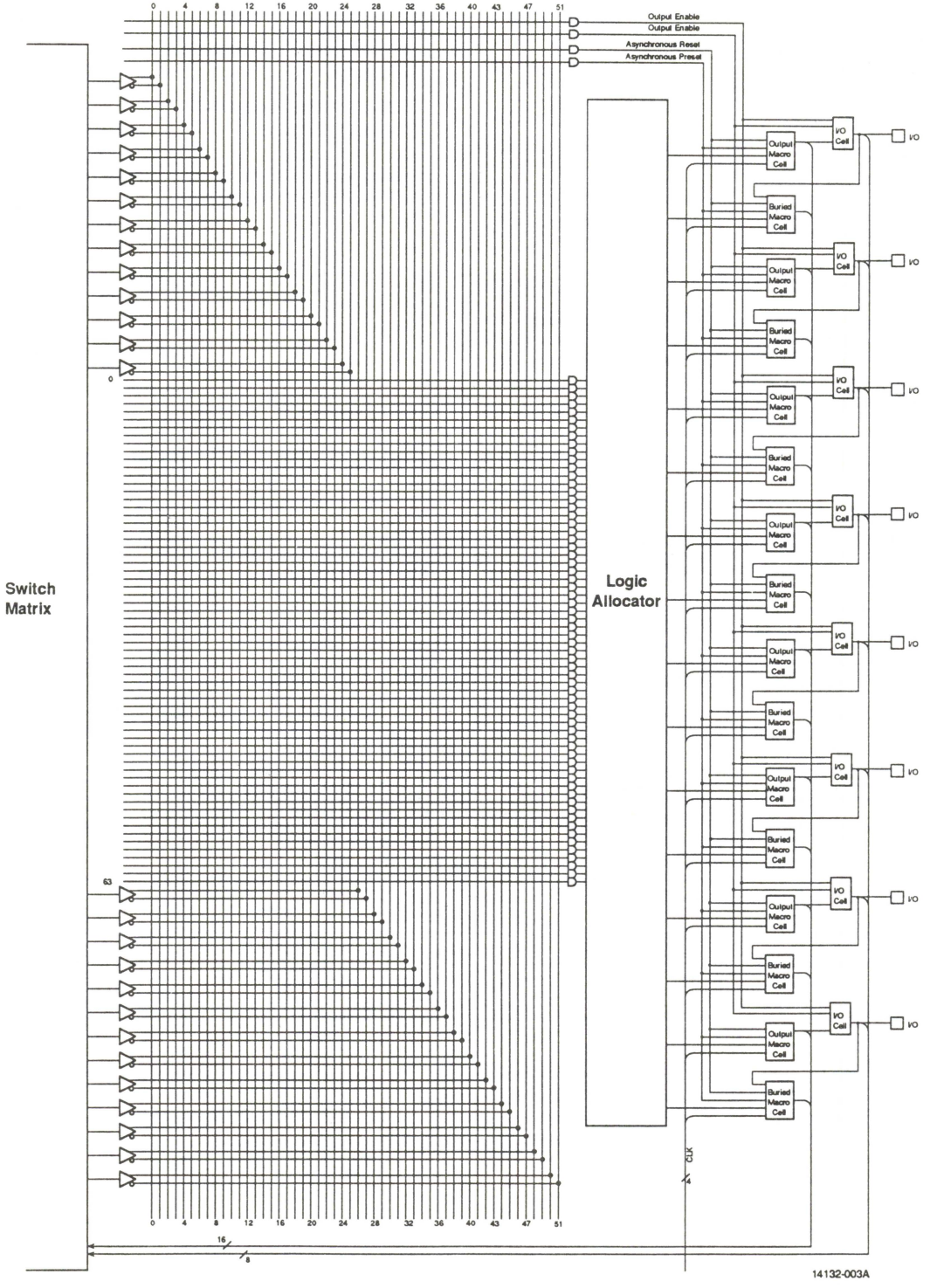


Figure 12. MACH230 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f =0 MHz		300	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz		pF

Note:
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	12		15		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	1/(t_S + t_{CO})	D-type	50		40		MHz
				T-type	45.5		37		MHz
		Internal Feedback		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	1/(t_{WL} + t_{WH})		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		13		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)				10		12		ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					17		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-Type	12		15		ns
				T-Type	14		17		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		1/(t_{WICL} + t_{WICH})		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				12		15		ns
t_{WIGZ}	Input Latch Gate Width LOW				6		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (Con'd)

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min.	Max.	Min.	Max.	
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	10		15		ns
t_{AP}	Asynchronous Preset to Registered Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)		15		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz			mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz		pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Register Data Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate						ns
t_{HL}	Latch Data Hold Time						ns
t_{GO}	Gate to Output (Note 3)						ns
t_{GWL}	Gate Width LOW						ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch						ns
t_{SIR}	Input Register Setup Time						ns
t_{HIR}	Input Register Hold Time						ns
t_{ICO}	Input Register Clock to Combinatorial Output						ns
t_{ICS}	Input Register Clock to Output Register Setup						ns
t_{WICL}	Input Register Clock Width			LOW			ns
t_{WICH}				HIGH			ns
f_{MAXIR}	Maximum Input Register Frequency (Note 4)		$1/(t_{WICL} + t_{WICH})$				MHz
t_{SIL}	Input Latch Setup Time						ns
t_{HIL}	Input Latch Hold Time						ns
t_{IGO}	Input Latch Gate to Combinatorial Output						ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch						ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate						ns
t_{IGS}	Input Latch Gate to Output Latch Setup						ns

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2) (Cont'd)

Parameter Symbol	Parameter Description	-20		Unit
		Min.	Max.	
t_{WIGZ}	Input, Latch Gate Width LOW			ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			ns
t_{AR}	Asynchronous Reset to Registered Output		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)			ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)			ns
t_{AP}	Asynchronous Preset to Registered Output		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)			ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)			ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)		20	ns

Notes:

2. See Switching Test Circuit, page 69, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

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Input/Output Equivalent Schematics 71
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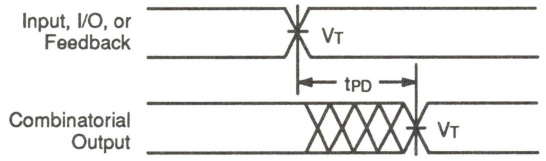
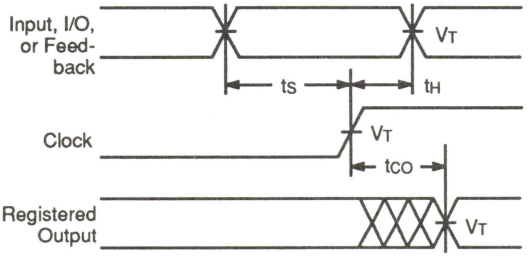
Programmer Socket Adapters 74
Development Systems 75
Physical Dimensions 76

SWITCHING WAVEFORMS



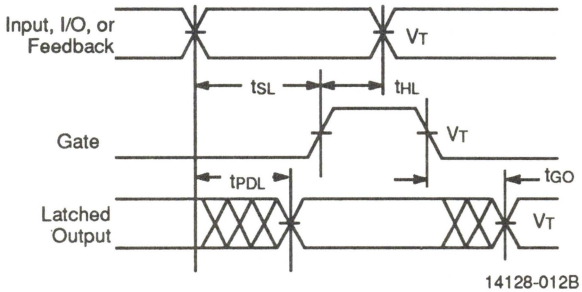
14128-010B

Combinatorial Output



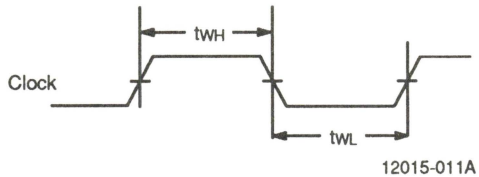
14128-011B

Registered Output



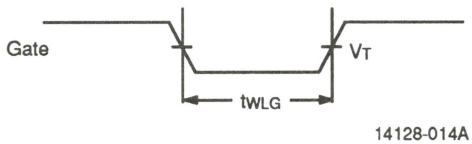
14128-012B

Latched Output (MACH 2 only)



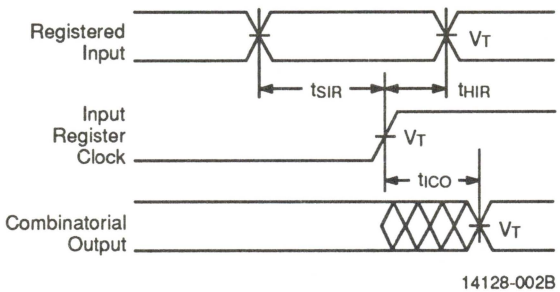
12015-011A

Clock Width



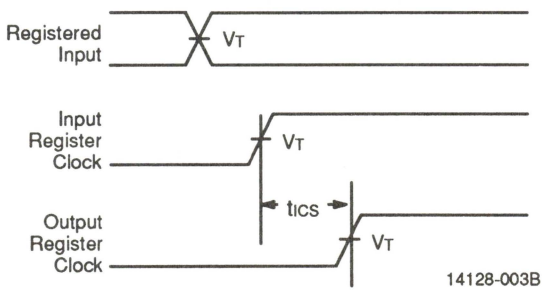
14128-014A

Gate Width (MACH 2 only)



14128-002B

Registered Input (MACH 2 only)



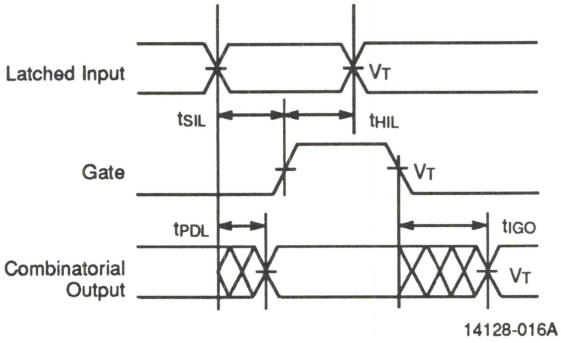
14128-003B

Input Register to Output Register Setup (MACH 2 only)

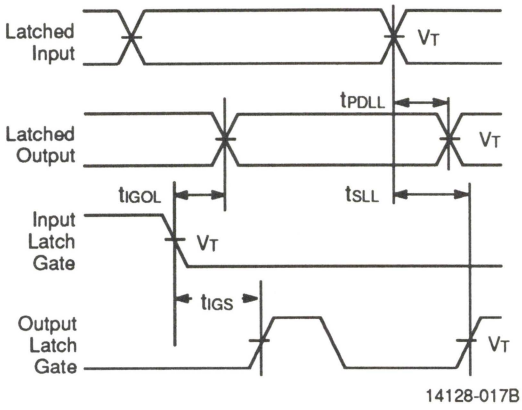
Notes:

1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

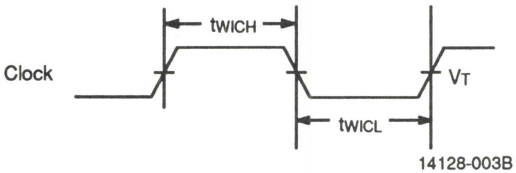
SWITCHING WAVEFORMS



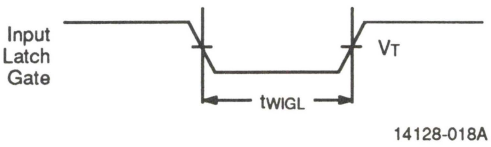
Latched Input (MACH 2 only)



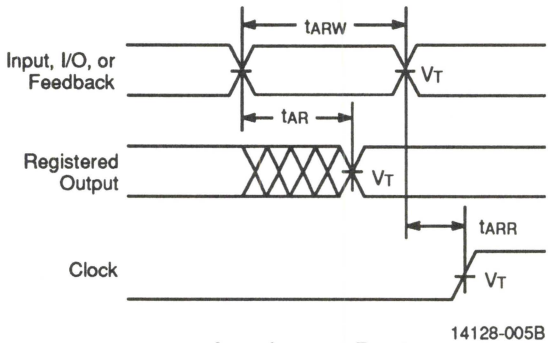
Latched Input and Output (MACH 2 only)



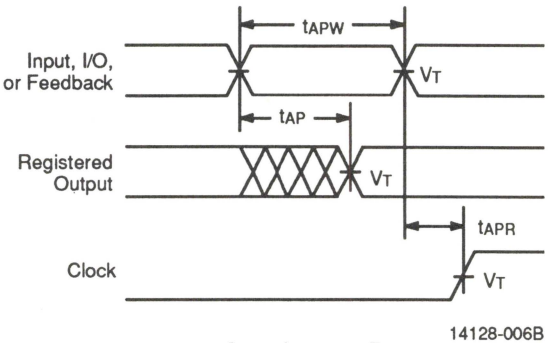
Input Register Clock Width (MACH 2 only)



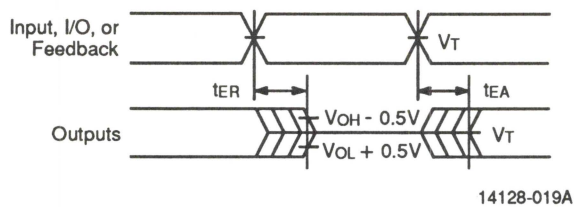
Input Latch Gate Width (MACH 2 only)



Asynchronous Reset



Asynchronous Preset



Output Disable/Enable

Notes:

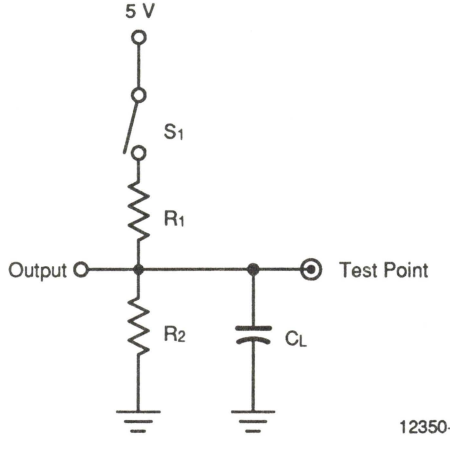
1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

			PRELIMINARY				
			Commercial		Military		Measured Output Value
Specification	S_1	C_L	R_1	R_2	R_1	R_2	
t_{PD}, t_{CO}, t_{CF}	Closed	35 pF	300 Ω	390 Ω	390 Ω	750 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed						1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF					H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} Parameters

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

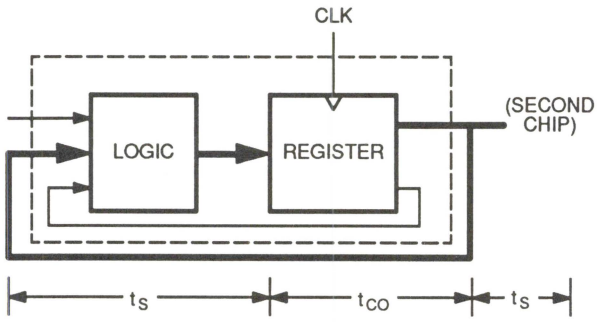
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal".

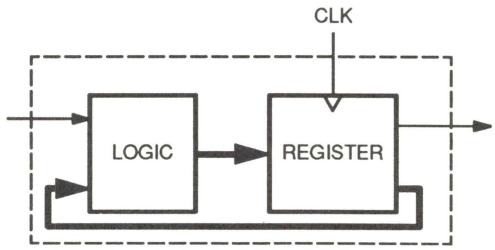
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$.

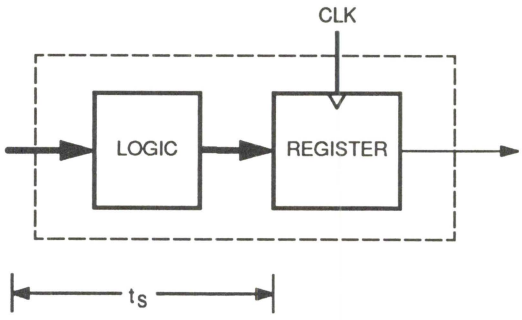
All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



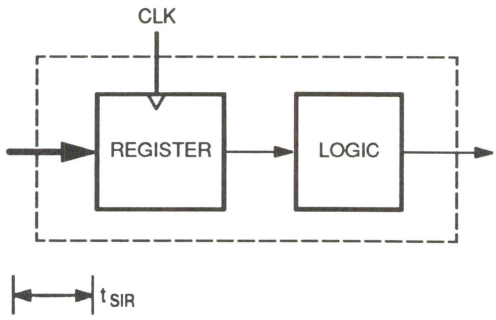
f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$



f_{MAXIR} ; $1/(t_{SIR} + t_{HIR})$ or $1/(t_{WICL} + t_{WICH})$

12350-023A

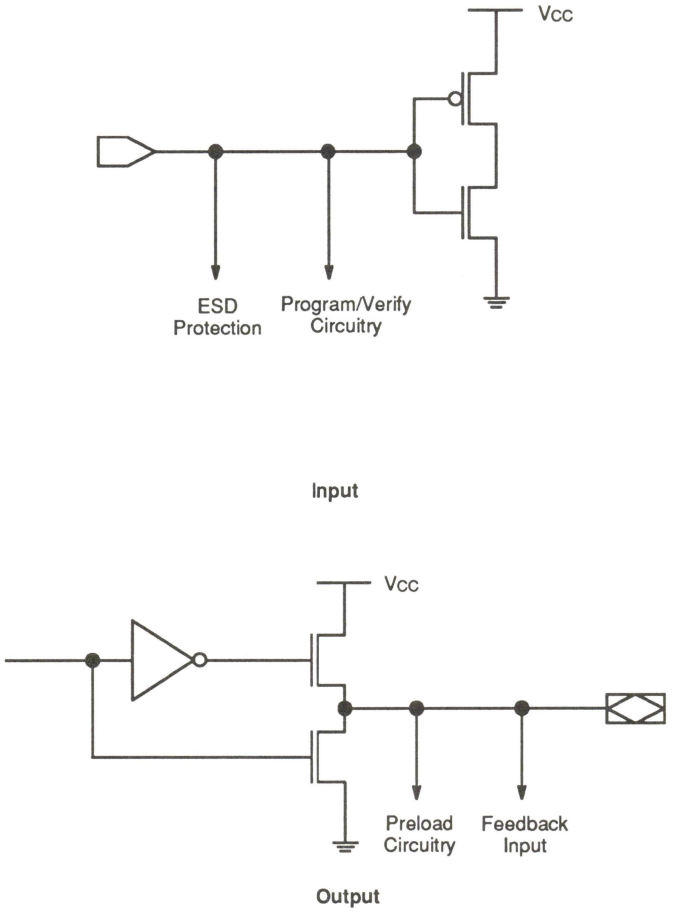
ENDURANCE CHARACTERISTICS

The MACH 1 and MACH 2 families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Endurance Characteristics

Parameter Symbol	Parameter Description	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



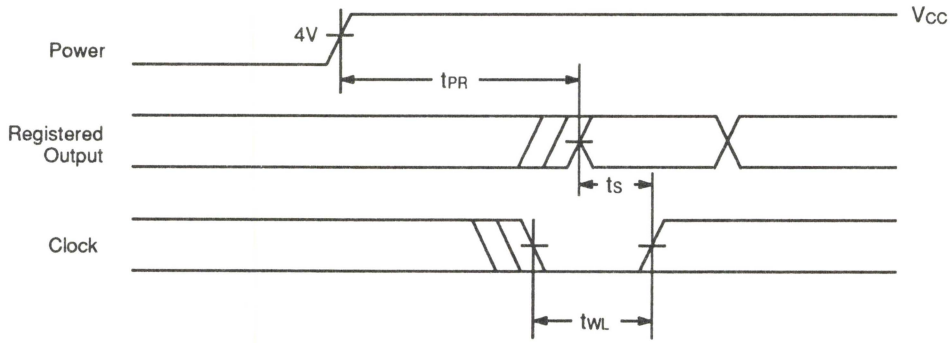
12197-013A

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max.	Unit
t_{PR}	Power-Up Reset Time	10	µs
ts	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



12350-024A

Power-Up Reset Waveform

APPROVED PROGRAMMERS (subject to change)

MANUFACTURER	PROGRAMMER CONFIGURATION	
Advanced Micro Devices 901 Thompson Pl. Sunnyvale, CA 94088 (800) 222-9323 or (408) 732-2400	LabPro™ (Note 1) MACH110: Rev. 1.2	
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (713) 461-9430	Model CP-1128 (Note 1) MACH110: Rev. 1.47 MACH210: Rev. 1.55	
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	UniSite™ (Note 2) MACH110: Rev. 3.2 MACH210: Rev. 3.3 Model 29 (Note 1) LogicPak™303A–011A MACH110: V14 MACH210: V15	Family-Pinout Codes: MACH110: 17F-0BD MACH210: 194-0C1 MACH110: 7F-BD MACH210: 4-C1
Digelec Inc. 20144 Plummer St. Chatsworth, CA 91311 (800) 367-8750 or (818) 701-9677 or 25 Galgaley Haplada St. Herzliya B46722, Israel 52-55-9615	Contact Manufacturer	
JMC Hakusan High-Tech Park 807-1 Hakusan-Cho Midori-Ku Yokohama-City 226, Japan 045-393-6150	Contact Manufacturer	
Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020 or Breslauer Str. 1 D-8057 Eching, Munich, Germany 8165-770	Contact Manufacturer	
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405	ALLPRO (Note 1) MACH110: Rev. 1.5	ALLPRO88 MACH110: Rev. 2.0
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Manufacturer	
Sprint Expert International, Inc. 13720 Midway Suite 105 Dallas TX 75244 (800) 688-3122 or (214) 233-3122 or Vanderweydendreef 27 1900 Overijse, Belgium 2-687-4154	Sprint (Note 1) MACH110: Rev. 3.4	
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	ZL30 (Note 1) MACH110: Rev. 41	Family-Pinout Codes: MACH110: 25253

Notes:

1. Requires socket adapter.
2. Requires 12 pin driver boards.

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System General 244 S. Hillview Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Contact Manufacturer

PROGRAMMER SOCKET ADAPTERS (subject to change)

MANUFACTURER	PART TYPE
CTI 14425 N. Scottsdale Rd. Suite 300 Scottsdale, AZ 85260 (602) 998–1484	PD1065-00
Emulation Technology 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982–0660	AS-44-28-01P-3TEX

DEVELOPMENT SYSTEMS (subject to change)

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM	
Advanced Micro Devices, Inc. P.O. Box 3453 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PALASM 4 Software MACH Libraries and Interface to OrCAD/SDT™ Software (Optional)	MACH110: Rev. 1.0 MACH210: Rev. 1.1
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 (800) 247-5700 or (206) 881-6444	ABEL™ Software Requires SmartPart™ MACH Fitter	MACH110: Rev. 4.0 MACH210: Rev. 4.0
ISDATA GmbH Haid-und-Neu-Str. 7 D-7500 Karlsruhe 1, Germany 0721/69 30 92 or (408) 373-7359 in U.S.	LOG/iC™ Software	MACH110: Rev. 4.0 MACH210: Rev. 4.0
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 491-7405	CUPL™ Software	MACH110: Rev. 3.3 MACH210: Rev. 3.3
Minc Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PGADesigner™ Software	MACH110: Rev. 2.1 MACH210: Rev. 2.1
OrCAD 1049 S.W. Baseline St., Suite 500 Hillsboro, OR 97123 (503) 640-9488	OrCAD/PLD™ Software	MACH110: Rev. 4.01 MACH210: Rev. 4.01
MANUFACTURER	**TEST GENERATION SYSTEM**	
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software	MACH110: Rev. 2.47 MACH210: Rev. 2.47
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 247-5700 or (206) 881-6444	PLDtest® Plus Software	
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OrCAD 1049 S.W. Baseline St., Suite 500 Hillsboro, OR 97123 (503) 640-9488	OrCAD/VST™	MACH110: Rev. 4.0 MACH210: Rev. 4.0

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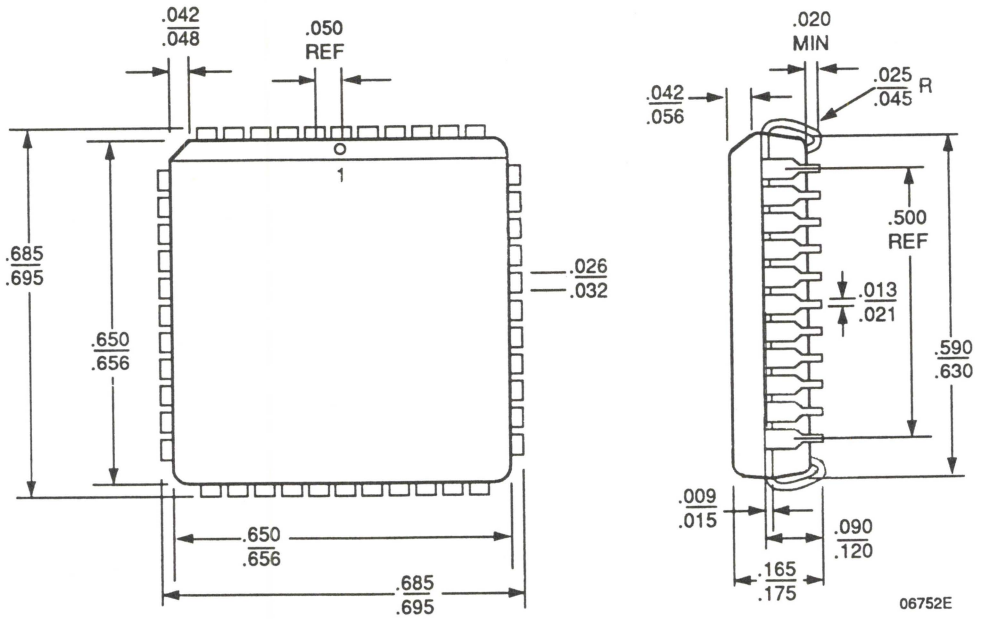
PHYSICAL DIMENSIONS*

PL 044
44-Pin Plastic Leaded Chip Carrier



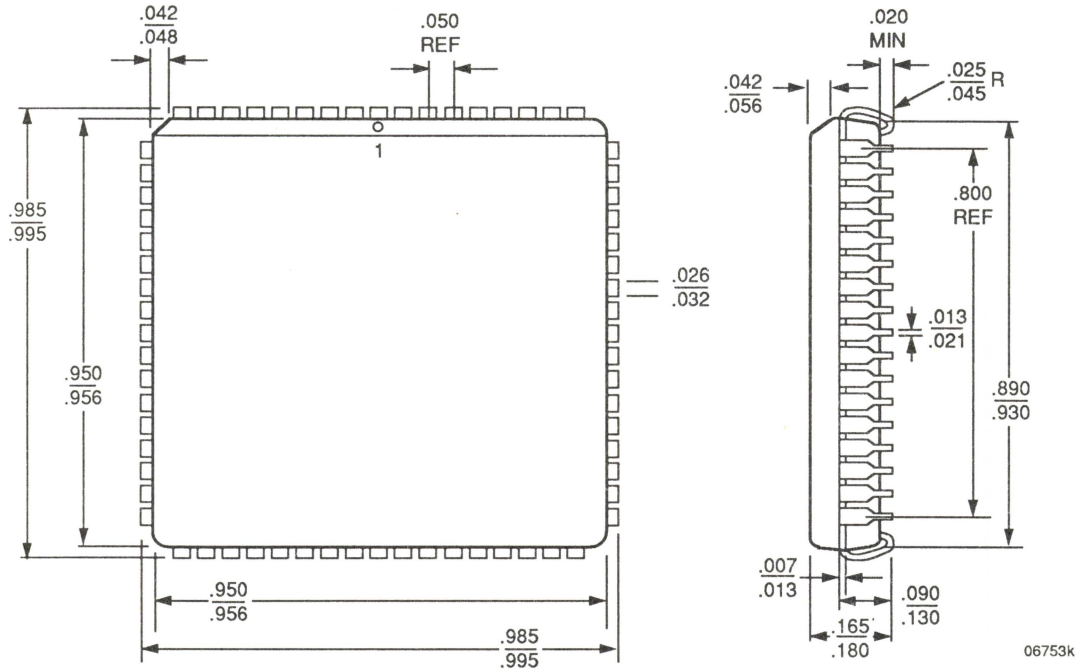
CQFP**
44-Pin Ceramic Quad Flatpack

* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Spacing Centering.
** Package in Development

PHYSICAL DIMENSIONS*

PL 068

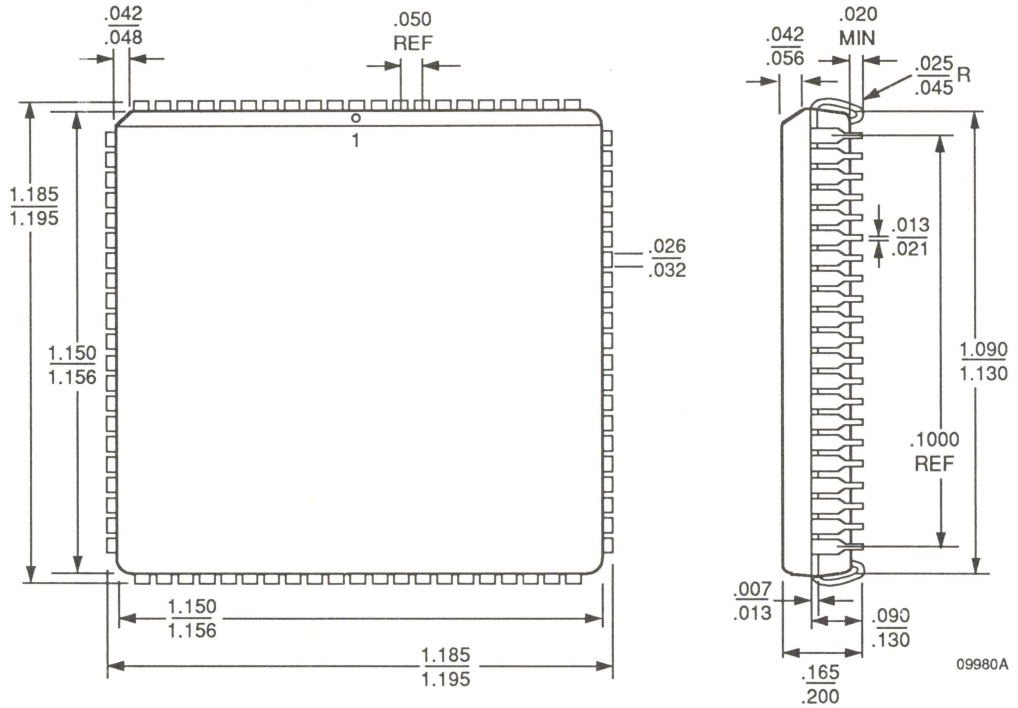
68-Pin Plastic Leaded Chip Carrier



PHYSICAL DIMENSIONS*

PL 084

84-Pin Plastic Leaded Chip Carrier



CQFP**

84-Pin Ceramic Quad Flatpack

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ADVANCED MICRO DEVICES, INC.
901 Thompson Place
P.O. Box 3453
Sunnyvale
California 94088-3453
(408) 732-2400
TWX: 910-339-9280
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